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PATENT ABSTRACTS OF JAPAN

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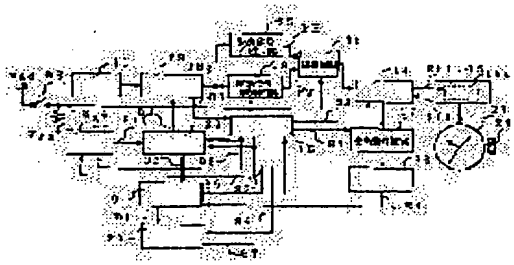
(54) DATA TRANSMITTING/RECEIVING SYSTEM FOR HAND TYPE ELECTRONIC TIMEPIECE

(57)Abstract:
PURPOSE: To provide a data transmitting/receiving system for hand type electronic timepiece.
CONSTITUTION: Output signals from a step signal generating circuit 25 and a drive signal generating circuit 13 are fed to a converter coil 15a while being switched by a switching circuit 26. Under communication function mode, a timing signal is fed from the step signal generating circuit to the converter coil 15a in order to perform bilateral communication. A 1Hz signal is stored at the time of designating the mode and the time is reset automatically at the end of mode.



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CLAIMS

[Claim(s)]

[Claim 1] In the data receiving system of the electronic clock which consists of the data source which generates a data signal, and an electronic clock which makes the coil for converters for an indicator drive serve a double purpose, and receives the data signal from the aforementioned data source A watch error signal generation means to generate a timing signal in the aforementioned electronic clock, and the driving-signal generating circuit which generates an indicator driving pulse, The electronic switch for changing a converter drive circuit, and the aforementioned timing signal generating means and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting, Have a terminal for a functional setup for controlling this electronic switch, and while controlling the aforementioned electronic switch by the aforementioned terminal for a functional setup and having set up function mode with it, the coil for the aforementioned converters is made to serve a double purpose. And the data transceiver system of the indicator formula electronic clock characterized by performing transceiver operation by making the aforementioned timing signal into a synchronizing signal.

[Claim 2] The data transceiver system of the indicator formula electronic clock according to claim 1 characterized by preparing the time return circuit which memorizes the indicator driving pulse generated while the aforementioned electronic switch has set up function mode, and the aforementioned electronic switch making rapid-traverse correction for an indicator according to the information on the aforementioned time return circuit at the time of a time mode return.

[Claim 3] The aforementioned time return circuit is the data transceiver system of the indicator formula electronic clock according to claim 2 which a timer means to set up function mode is established, and the aforementioned time return circuit operates by the terminate signal of this timer means of operation, and makes rapid-traverse

correction for an indicator.

[Claim 4] The oscillator circuit and a watch error adjustment means to adjust the frequency of the output signal of this oscillator circuit which are characterized by providing the following, A watch error adjustment data-storage means to memorize the watch error adjustment data of this watch error adjustment means, The driving-signal generating circuit which generates an indicator driving pulse, and a converter drive circuit, The indicator formula electronic clock equipped with the coil for converters driven by the output signal of this converter drive circuit, Detect a signal and watch error measurement is performed. the criteria which have the periodicity generated from the coil for converters of this indicator formula electronic clock -- electromagnetism -- the measurement result -- the watch error adjustment data of an indicator formula electronic clock -- creating -- the watch error adjustment data -- adjustment -- electromagnetism -- the watch error regulating system constituted by the watch error adjusting device which makes a signal and is outputted to the aforementioned indicator formula electronic clock The aforementioned indicator formula electronic clock is a watch error signal generating circuit which generates the pulse for watch error measurement. The electronic switch for changing this watch error signal generating circuit and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting. The watch error measurement specification terminal for controlling this electronic switch.

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the data transceiver system of an indicator formula electronic clock.

[0002]

[Description of the Prior Art] Although there is a watch error adjustment function as an example of the setting up function in an electronic clock conventionally, this watch error adjustment method has the thing in use which measures the period of the watch error signal outputted from an electronic clock, supplies the amount of watch error adjustments in digital one using an input terminal from the exterior by making a difference with a criteria period into the amount of watch error adjustments, and consists of non-volatile memory etc. and which a note of is made and the circuit is made to memorize. Moreover, the indicator formula electronic clock which receives an allowed-time signal from external allowed-time signal generation equipment as an example of a data receiving system which makes the coil for converters for an indicator drive serve a double purpose in an indicator formula electronic clock, and receives a

signal, and performs watch error adjustment is proposed. (For example, JP,58-7190,B) In order that this clock may receive the allowed-time signal in a cycle of [from the outside] 1 second, it waits to set up a receiving state by operation of external actuator material, such as RYUZU, to change a frequency divider into a reset state simultaneously, and to input an allowed-time signal. If the allowed-time signal of the 1st shot is inputted, reset of a frequency divider will be canceled and a frequency deviation measuring circuit will start a count. And if the allowed-time signal of the 2nd shot is inputted after 1 second, while stopping a count, a frequency deviation store circuit is made to memorize the frequency deviation which the aforementioned frequency deviation measuring circuit counted, and automatic watch error adjustment is ended. And reset is applied again, reset is automatically canceled after fixed time, and normal operation is started. namely, the allowed-time signal in a cycle of [which is supplied from the outside in the above-mentioned operation / exact] 1 second -- an internal counter -- counting -- carrying out -- the enumerated data -- as the period of 1 future second -- a time check -- it is the one-sided receiving method which operates, and the coil for converters is used for reception of the allowed-time signal

[0003]

[Problem(s) to be Solved by the Invention] The above-mentioned method can perform watch error adjustment also in a completion clock, and is a very convenient method. However, while this watch error adjustment method, on the other hand, sends the allowed-time signal of for example, a 1-second interval into a target from external allowed-time signal generation equipment regardless of the watch error of an indicator formula electronic clock, and counting of it is carried out, it memorizes the enumerated data with the frequency of the oscillator circuit which builds in the 1-second interval signal received in the indicator formula electronic clock side and it is henceforth said for 1 second by the enumerated data that it creates a signal, it is a write-in method of the tropism. However, by the above-mentioned method, since many memorandum ** corresponding to the enumerated data for 1 second are needed as a watch error adjustment data storage means, in the wrist watch for which the low consumed electric current is needed, it is not adopted by small. The method which performs a good variations periphery or changes the capacity of an oscillator circuit by time sharing using memory space few as a watch error adjustment means adopted with the present electronic wrist watch is adopted. Moreover, in order to set up a receiving state by operation of external actuator material, such as RYUZU, in order to receive an allowed-time signal, and to change a frequency divider into a reset state simultaneously, operation as a clock will be in a idle state. Therefore, after performing watch error

adjustment, it is necessary to carry out time doubling again. The purpose of this invention offers the data transceiver system of the indicator formula electronic clock which performs two-way communication by making the timing signal from an electronic clock into a synchronizing signal. And the indicator driving pulse generated in the state of reception is memorized, and the data transceiver system of the indicator formula electronic clock which made rapid-traverse correction and made time correction unnecessary after the reception end is offered. The data transceiver system which can be adapted for the watch error adjustment means using the further above-mentioned few capacity memory is offered.

[0004]

[Means for Solving the Problem] In order to make the above-mentioned purpose attain, this invention is considered as the following composition. In the data transceiver system of the electronic clock which consists of the data source which generates a data signal, and an electronic clock which makes the coil for converters for an indicator drive serve a double purpose, and receives the data signal from the aforementioned data source A timing signal generating means to generate a timing signal in the aforementioned electronic clock, The driving-signal generating circuit which generates an indicator driving pulse, and a converter drive circuit, The electronic switch for changing the aforementioned timing signal generating means and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting, It is characterized by having a terminal for a functional setup for controlling this electronic switch, making the coil for converters serve a double purpose, while controlling the aforementioned electronic switch by the aforementioned terminal for a functional setup and having set up function mode with it, and performing transceiver operation by making the aforementioned timing signal into a synchronizing signal.

[0005] Furthermore, the time return circuit which memorizes the indicator driving pulse generated while the aforementioned electronic switch has set up function mode is prepared, and it is characterized by the aforementioned electronic switch making rapid-traverse correction for an indicator according to the information on the aforementioned time return circuit at the time of a time mode return.

[0006] Furthermore, it is characterized by establishing a timer means to set up function mode, for the aforementioned time return circuit operating by the terminate signal of this timer means of operation, and the aforementioned time return circuit making rapid-traverse correction for an indicator.

[0007] Furthermore, an oscillator circuit and a watch error adjustment means to adjust the frequency of the output signal of this oscillator circuit, A watch error adjustment

data-storage means to memorize the watch error adjustment data of this watch error adjustment means, The driving-signal generating circuit which generates an indicator driving pulse, and a converter drive circuit, The indicator formula electronic clock equipped with the coil for converters driven by the output signal of this converter drive circuit, Detect a signal and watch error measurement is performed. the criteria which have the periodicity generated from the coil for converters of this indicator formula electronic clock -- electromagnetism -- It is the watch error regulating system constituted by the watch error adjusting device which makes a signal and is outputted to the aforementioned indicator formula electronic clock. the measurement result -- the watch error adjustment data of an indicator formula electronic clock -- creating -- the watch error adjustment data -- adjustment -- electromagnetism -- The watch error signal generating circuit in which the aforementioned indicator formula electronic clock generates the pulse for watch error measurement, Having had the watch error measurement specification terminal for controlling the electronic switch and this electronic switch for changing this watch error signal generating circuit and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting is characterized by things.

[0008]

[Example] The example which was adapted for the watch error adjustment function in the transceiver system of this invention with the drawing below is explained. Drawing 1 is the block diagram of the watch error regulating system of the indicator formula electronic clock equipped with the watch error adjustment function which shows the first example in this invention. 1 is the indicator formula electronic clock equipped with the correction switch RS which is interlocked with RYUZU 24 for stopping coil 15a for converters for driving an indicator, and an indicator drive, and correcting time, and operates. 2 is a watch error adjusting device and is equipped with the coil 31 for transmission and reception. The aforementioned coil 31 for transmission and reception transmits and receives between the aforementioned coil 15a for converters. the criteria which the aforementioned watch error adjusting device 2 generates from coil 15for converters a at the time of time correction of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- a signal S40 -- the aforementioned coil 31 for transmission and reception -- receiving -- watch error measurement -- carrying out -- the measurement result -- the watch error adjustment data of an indicator formula electronic clock 1 -- creating -- the aforementioned criteria -- electromagnetism -- a signal S40 -- synchronizing -- the aforementioned watch error adjustment data -- adjustment -- electromagnetism -- it considers as a signal 41 and it transmits

[0009] Drawing 2 is the circuit block diagram of the indicator formula electronic clock 1 in this invention. 11 is an oscillator circuit which makes a quartz resonator a reference signal, and 12 is a frequency divider which outputs 1Hz signal and the dividing signal S1 for creating an indicator driving pulse by considering the oscillation signal from an oscillator circuit 11 as an input. 13 is a driving-signal generating circuit and outputs the pulse PM for an indicator drive to the converter drive circuit 14 as a signal which considers 1Hz signal from a frequency divider 12 as an input, and drives a motor. 15a has the function as a coil for transmission and reception to be the coil for converters with which the converter 15 for driving the indicator driving gear 23 was equipped, and to perform transmission and reception with the aforementioned watch error adjusting device 2. 24 is RYUZU for correcting the time of the indicator driving gear 23, and is in zero step of position in a normal state. By lengthening one step of RYUZU 24, Switch RS is a correction switch which interlocks and operates, has a function as a watch error measurement specification terminal, and forbids the pulse PM output for an indicator drive from the driving-signal generating circuit 13. 25 is a watch error signal generating circuit, considers 1Hz signal from a frequency divider 12 as an input, and outputs the pulse PH for watch error measurement of the pulse width which is the grade which is a period of 1 second and a stepping motor does not drive to the converter drive circuit 14.

[0010] 26 is an electronic switch which considers the pulse PM for an indicator drive, and the pulse PH for watch error measurement as an input, chooses the pulse PM for an indicator drive in a normal state, chooses the pulse PH for watch error measurement in the state of the correction which lengthened one step of RYUZU 24, and is outputted to the converter drive circuit 14. The pulse PH for watch error measurement outputted from the watch error signal generating circuit 25 in this example serves as a timing signal transmitted to the aforementioned watch error adjusting device 2, therefore the watch error signal generating circuit 25 has a function as a timing signal generating circuit. if, as for the aforementioned coil 15a for converters, the pulse PH for watch error measurement is supplied -- criteria -- electromagnetism -- a signal S40 is generated 16 is a control signal generating circuit, inputs the aforementioned dividing signal S1, and outputs many control signals of the ready-for-receiving ability signal S2 grade which changes the aforementioned converter drive circuit 14 into a receiving state. the detection enabling signal S3 which 17 is a detection permission circuit and is outputted from the aforementioned control signal generating circuit 16 -- adjustment -- electromagnetism -- passage of the input signal S12 from coil 15for converters a which received the signal S41 is forbidden or permitted 18 is a watch error adjustment signal-detection circuit, and changes into watch error adjustment signal S4 the input

signal S12 which passed through the aforementioned detection permission circuit 17. 19 is a shift register, memorizes watch error adjustment signal S4 from the watch error adjustment signal-detection circuit 18 with the data shift signal S5 outputted from the aforementioned control signal generating circuit 16, and outputs a data signal D1 and a data signal D2.

[0011] It judges whether the data signal D1 of 20 memorized with the aforementioned shift register 19 by the data judging signal S6 which is a rewriting judging circuit and is outputted from the aforementioned control signal generating circuit 16 is effective, and if right, the data rewriting enabling signal S7 will be outputted to the aforementioned control signal generating circuit 16. 21 is a booster circuit, the elimination signal S8 and write-in signal S9 which are outputted from the aforementioned control signal generating circuit 16 perform pressure-up operation, and only fixed time outputs the pressure-up signal S10. 22 is the amount store circuit of watch error adjustments which consists of non-volatile memory etc., and when the data signal D2 from the aforementioned shift register 19 and the pressure-up signal S10 from a booster circuit 21 are considered as an input and elimination of data and writing are performed by the elimination signal S8 and write-in signal S9 which are outputted from the aforementioned control signal generating circuit 16, it supplies the watch error data D3 to the aforementioned frequency divider 12.

[0012] the watch error adjusting device [in / this example / a view 3 is a circuit block diagram of the watch error adjusting device 2 in this invention, and] 2 -- the criteria from the aforementioned indicator formula electronic clock 1 -- electromagnetism -- the watch error adjustment data which receive a signal S40 as a watch error detecting signal, perform watch error measurement based on this, and follow the result -- adjustment -- electromagnetism -- it is the watch error adjusting device transmitted as a signal 41 31 is the aforementioned coil for transmission and reception. the change signal S21 from the transceiver control circuit 39 which 32 is a transceiver electronic switch and is mentioned later -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- receiving a signal S40 **** -- coil 15a for converters -- adjustment -- electromagnetism -- change control of transmitting a signal 41 is carried out 33 -- a gate circuit -- it is -- the aforementioned criteria -- electromagnetism -- passage of a signal S40 is forbidden or permitted 34 is a watch error signal-detection circuit, and consists of filter circuit 34a and amplifying-circuit 34b -- having -- the criteria from the aforementioned gate circuit 33 -- electromagnetism -- a signal S40 is inputted and it detects as a watch error detection pulse PT 35 is a period-measurement circuit, considers the aforementioned watch error detection pulse PT as an input, measures the

interval of two or more watch error detection pulses PT with the reference signal S13 from the reference signal generating circuit 36, and outputs measurement data D4.

[0013] at the same time it outputs the system clear signal S22 which 37 is a measurement start store circuit and initializes the watch error adjusting device 2 by operation of a switch 38 -- the receiving enabling signal S23 -- outputting -- the aforementioned gate circuit 33 -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- it is controlling to permit passage of a signal S40 39 is a transceiver control circuit and outputs many control signals of the change signal S21 grade which considers the aforementioned watch error detection pulse PT as an input, and makes the aforementioned transceiver electronic switch 32 a send state. 47 is the 1st data-storage circuit, it considers measurement data D4 from the aforementioned period-measurement circuit 35 as an input, memorizes the aforementioned measurement data D4 with the periodic latch signal S31 outputted whenever the aforementioned transceiver control circuit 39 inputs the aforementioned watch error detection pulse PT, and outputs the periodic stored data D8. 48 is the 2nd data-storage circuit, newly memorizes the aforementioned periodic stored data D8 with the NG signal S34 outputted from the comparison-test circuit 49 which considers the periodic stored data D8 from the aforementioned 1st data-storage circuit 47 as an input, and mentions it later, and outputs it as periodic criteria data D9. the value which 49 is a comparison-test circuit, considered the aforementioned periodic stored data D8 and the aforementioned periodic criteria data D9 as an input, and carried out the comparison test of the aforementioned periodic stored data D8 and the aforementioned periodic criteria data D9 with the comparison signal S32 outputted from the aforementioned transceiver control circuit 39, outputted an O.K. signal S33 to the aforementioned transceiver control circuit 39, and compared it when the value which compared was specification within the limits -- specification -- if out of range, an NG signal S34 will output to the

[0014] 41 is the amount arithmetic circuit of watch error adjustments, and the operation of the amount of watch error adjustments is started by the operation instruction signal S24 which inputs the aforementioned periodic stored data D8, and is outputted from the aforementioned transceiver control circuit 39. After an operation is completed, while outputting the amount data D5 of adjustments, the operation terminate signal S25 is outputted to the aforementioned transceiver control circuit 39. 42 is a transmit data creation circuit, inputs the amount data D5 of adjustments from the aforementioned amount arithmetic circuit 41 of watch error adjustments, and changes them into the data signal D6 of binary code form. 43 is a rewriting command creation circuit and

creates the data signal D7 of the meaning of transmitting a data signal D6 after this, to the indicator formula electronic clock 1. 45 is a display circuit, considers the amount data D5 of adjustments from the aforementioned amount arithmetic circuit 41 of watch error adjustments as an input, and consists of a conversion circuit changed into ppm or sunlight to a reference value, and a drive circuit which drives the display 46 equipped with LCD etc. It is a number-of-times counting circuit of NG, 50 inputs the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and if it counts and becomes more than the number of times with a fixed count (for example, 5 times), it will output a reset signal S35. This reset signal S35 clears and initializes the aforementioned measurement start store circuit 37 and a display circuit 45.

[0015] 44 is a data sending circuit and outputs the sending signal S28 which serial-data-ized the aforementioned data signal D7 and the data signal D6 by the clock signal S27 which is latched with the latch signal S26 which considers the aforementioned data signal D6 and a data signal D7 as an input, and is outputted from the aforementioned transceiver control circuit 39, and is outputted from the clock generation circuit 40 mentioned later. this sending signal S28 -- the aforementioned coil 31 for transmission and reception -- adjustment -- electromagnetism -- it is transmitted to the aforementioned indicator formula electronic clock 1 as a signal S41 40 is a clock generation circuit and outputs the clock signal S27 which drives the aforementioned data sending circuit 44 by the seizure signal S29 outputted from the aforementioned transceiver control circuit 39. moreover -- at the same time the transmitting terminate signal S30 outputted from the aforementioned transceiver control circuit 39 resets the aforementioned measurement start store circuit 37 and it initializes the watch error adjusting device 2 -- the aforementioned gate circuit 33 -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- passage of a signal S40 is forbidden

[0016] Next, operation of the watch error regulating system of the indicator formula electronic clock 1 equipped with the watch error adjustment function in the above-mentioned composition is explained according to the timing diagram of drawing 4 . The normal operation of the aforementioned indicator formula electronic clock 1 has RYUZU 24 in zero step of position, and the aforementioned change circuit 26 chooses and outputs motor driving pulse PM. By outputting the converter driving signal S11 and supplying coil 15a for converters, converter coil 15a drives the indicator driving gear 23, and the converter drive circuit 14 which inputs this motor driving pulse PM performs a time stamp by movement for 1 second. In the state of correction, 1 stage length of RYUZU 24 is carried out, the correction switch RS with which RYUZU 24 is

interlocked with and it operates will be in ON state, and a correcting signal S14 will be outputted. Forbidding the pulse PM output for an indicator drive from the aforementioned driving-signal generating circuit 13 by this correcting signal S14, the aforementioned change circuit 26 chooses and outputs the pulse PH for watch error measurement simultaneously. supplying this pulse PH for watch error measurement to coil 15a for converters -- coil 15a for converters -- criteria -- electromagnetism -- a signal S40 occurs the aforementioned control signal generating circuit 16 inputting the dividing signal S1 from the back frequency divider 12 with which the pulse PH for watch error measurement was outputted, and outputting the ready-for-receiving ability signal S2 -- the adjustment from the watch error adjusting device 2 -- electromagnetism -- the converter drive circuit 14 is changed to a receiving state so that a signal S41 can be received by coil 15a for converters Simultaneously, the aforementioned control signal generating circuit 16 outputs the detection enabling signal S3, and permits passage of an input signal S12 to the detection permission circuit 17. this -- the indicator formula electronic clock 1 -- the first pulse PH for watch error measurement -- criteria -- electromagnetism -- after outputting as a signal S40, only the time of the ready-for-receiving ability signal S2 is held in the ready-for-receiving ability state before the following pulse PH output for watch error measurement

[0017] on the other hand -- the watch error adjusting device 2 -- the criteria of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- in order to receive a signal S40, it initializes by operation of a switch 38 first The aforementioned measurement start store circuit 37 outputs the system clear signal S22 and the receiving enabling signal S23 by operation of this switch 38. with the system clear signal S22, the transceiver electronic switch 32 changes the receive mode -- having -- the criteria from the aforementioned indicator formula electronic clock 1 -- electromagnetism -- it changes into the receiving state where a signal S40 is receivable Simultaneously, the aforementioned rewriting command creation circuit 43 creates and outputs a data signal D7 with the system clear signal S22. The aforementioned period-measurement circuit 35, the aforementioned 2nd data-storage circuit 48, and the number-of-times counting circuit 50 of NG are cleared simultaneously. further -- the receiving enabling signal S23 from the aforementioned measurement start store circuit 37 -- a gate circuit 33 -- controlling -- the criteria from the aforementioned coil 31 for transmission and reception -- electromagnetism -- passage of a signal S40 is permitted this state -- the criteria of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- if a signal S40 is received, an input signal will pass a gate circuit 33 and will input it into the watch error signal-detection circuit 34 -- having -- this watch

error signal-detection circuit 34 -- the first criteria -- electromagnetism -- the watch error detection pulse PT which is a signal S40 is detected (Timing of the drawing 4 timing diagram t1)

[0018] The period-measurement circuit 35 ends the count of the reference signal S13 from the reference signal generating circuit 36 counted by t1 until now the time of the first watch error detection pulse PT 1 being inputted, outputs it as measurement data D4 (the first value is not right), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 1 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage circuit 47 memorizes the measurement data D4 at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8. Next, the aforementioned transceiver control circuit 39 outputs the comparison signal S32. With this comparison signal S32, the aforementioned comparison-test circuit 49 compares the aforementioned periodic stored data D8 with the aforementioned periodic criteria data D9 (the first value is 0) outputted from the 2nd data-storage circuit 48, and the NG signal S34 is outputted. The 2nd data-storage circuit 48 memorizes the aforementioned periodic stored data D8 as new periodic criteria data D9 with this NG signal S34. . Simultaneously, the aforementioned number-of-times counting circuit 50 of NG counts the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and the number of times of a count is set to 1.

[0019] next, the criteria of the indicator formula electronic clock 1 to a degree -- electromagnetism -- a signal S40 outputs -- having -- these criteria -- electromagnetism -- the 2nd watch error detection pulse PT 2 outputs from the aforementioned watch error signal-detection circuit 34 by receiving a signal S40 with the aforementioned coil 31 for transmission and reception -- having (timing of the drawing 4 timing diagram t2) -- The period-measurement circuit 35 ends the count of the reference signal S13 counted from t1 the time of the first watch error detection pulse PT 1 being inputted, outputs it as measurement data D4 (period T1 of the drawing 4 timing diagrams t1 and t2), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 2 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage circuit 47 memorizes the measurement data D4 (T1) at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8 (T1). Next, the aforementioned transceiver control circuit 39 compares the aforementioned periodic criteria data D9 to which the comparison signal S32 is

outputted and the aforementioned comparison-test circuit 49 is outputted by this comparison signal S32 from the aforementioned periodic stored data D8 and the 2nd data-storage circuit 48, and outputs the NG signal S34. With this NG signal S34, the 2nd data-storage circuit 48 memorizes the aforementioned periodic stored data D8 as new periodic criteria data D9 (T1), simultaneously, the aforementioned number-of-times counting circuit 50 of NG counts the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and the number of times of a count is set to 2.

[0020] further -- the criteria from the indicator formula electronic clock 1 -- electromagnetism -- a signal S40 outputs -- having -- these criteria -- electromagnetism -- the 3rd watch error detection pulse PT 3 outputs from the aforementioned watch error signal-detection circuit 34 by receiving a signal S40 with the aforementioned coil 31 for transmission and reception -- having (timing of the drawing 4 timing diagram t3) -- The period-measurement circuit 35 ends the count of the reference signal S13 counted from t2 the time of the watch error detection pulse PT 2 being inputted, outputs it as measurement data D4 (period T2 of the drawing 4 timing diagrams t2 and t3), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 3 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage circuit 47 memorizes the measurement data D4 (T2) at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8 (T2). Next, since the value which compared and compared the aforementioned periodic criteria data D9 (T1) to which the aforementioned transceiver control circuit 39 outputs the comparison signal S32, and the aforementioned comparison-test circuit 49 is outputted by this comparison signal S32 from the aforementioned periodic stored data D8 (T2) and the 2nd data-storage circuit 48 is specification within the limits, the O.K. signal S33 is outputted to the aforementioned transceiver control circuit 39, and the aforementioned transceiver control circuit 39 outputs the operation-instruction signal S24.

[0021] If this operation instruction signal S24 is outputted to the amount arithmetic circuit 41 of watch error adjustments, the amount arithmetic circuit 41 of watch error adjustments will start the operation of the amount of watch error adjustments from the aforementioned periodic stored data D8 (T2), and after an operation is completed, while outputting the amount data D5 of adjustments which are the result of an operation, the operation terminate signal S25 is outputted to the aforementioned transceiver control circuit 39. The amount data D5 of adjustments outputted from the aforementioned amount arithmetic circuit 41 of watch error adjustments are changed into the data

signal D6 of binary code form in the transmit data creation circuit 42. Moreover, the amount data D5 of adjustments are simultaneously changed into sunlight by the display circuit 45, and the value is displayed on display 46. If the aforementioned operation terminate signal S25 is outputted to the aforementioned transceiver control circuit 39, the transceiver control circuit 39 will output the latch signal S26, and will memorize the aforementioned data signal D7 and a data signal D6 to the data sending circuit 44. Moreover, the change signal S21 is outputted synchronizing with the aforementioned watch error detection pulse PT 3 (drawing 4 timing diagram t4), and the transceiver electronic switch 32 is set as a send state. And by the clock signal S27 from the clock generation circuit 40 which operates by the seizure signal S29 outputted to a degree from the transceiver control circuit 39, the data signal D7 and data signal D6 which are memorized by the data sending circuit 44 are outputted one by one as a sending signal S28. A sending signal S28 is transmitted to the aforementioned indicator formula electronic clock 1 as an adjustment signal S41 through the transceiver electronic switch 32 and the coil 31 for transmission and reception. If it finishes transmitting a sending signal S28 altogether, the transceiver control circuit 39 will output the transmitting terminate signal S30.

[0022] The timing to which a series of aforementioned sending signals S28 are transmitted suits the state, i.e., the receiving state of the indicator formula electronic clock 1, where the control signal generating circuit 16 of the indicator formula electronic clock 1 is outputting the ready-for-receiving ability signal S2 as shown in the change signal S21 of the timing diagram of drawing 4 , and the ready-for-receiving ability signal S2 of the aforementioned indicator formula electronic clock 1. The transmitting terminate signal S30 from the aforementioned transceiver control circuit 39 is inputted into the aforementioned measurement start store circuit 37, and the receiving enabling signal S23 stops and it has the aforementioned gate circuit 33 closed by resetting this measurement start store circuit 37. One watch error adjustment operation is completed above, and it is resumed by pushing a switch 38 to perform watch error adjustment operation again.

[0023] The adjustment MAG signal S41 transmitted from the aforementioned watch error adjusting device 2 on the other hand explains the operation below, although received by coil 15a for converters of the indicator formula electronic clock 1. The aforementioned indicator formula electronic clock 1 is the ready-for-receiving ability signal S2 which the control signal generating circuit 16 outputs, changes the converter drive circuit 14 to a receiving state, and receives the adjustment MAG signal S41 which consisted of a data signal D7 transmitted from the watch error adjusting device 2, and a

data signal D6 as an input signal S12 by coil 15a for converters. The input signal S12 which received is detected through the detection permission circuit 17 in the watch error adjustment signal-detection circuit 18, and is outputted as a watch error adjustment signal S4. After a shift register 19 memorizes one by one by the data shift signal S5 which the control signal generating circuit 16 outputs and all storage of the watch error adjustment signal S4 is completed, the detected watch error adjustment signal S4 makes the aforementioned data signal D7 a data signal D1, is outputted to the aforementioned rewriting judging circuit 20, and outputs to the aforementioned watch error adjustment store circuit 22 by making the aforementioned data signal D6 into a data signal D2. The control signal generating circuit 16 will output the data judging signal S6 to the aforementioned rewriting judging circuit 20, if it finishes outputting the data shift signal S5, and it judges whether it is effective, and if the data signal D1 is effective, as for this rewriting judging circuit 20, it will output the data rewriting enabling signal S7. However, when the judgment result in the aforementioned rewriting judging circuit 20 is invalid, the data rewriting enabling signal S7 is not outputted, and watch error adjustment is not performed.

[0024] The control signal generating circuit 16 will output the elimination signal S8, if the data rewriting enabling signal S7 is inputted, it sets the amount store circuit 22 of watch error adjustments as elimination mode, operates a booster circuit S21 simultaneously, and eliminates the data of the amount store circuit 22 of watch error adjustments with the pressure-up signal S10. Then, the control signal generating circuit 16 outputs the write-in signal S9, and watch error adjustment ends it by setting the amount store circuit 22 of watch error adjustments as write-in mode, operating a booster circuit 21 simultaneously, and writing the data signal D2 which is the amount data of adjustments in the amount store circuit 22 of watch error adjustments with the pressure-up signal S10.

[0025] Drawing 5 is the circuit block diagram of the indicator formula electronic clock 1 of the second example in this invention. this example sets up the ready-for-receiving ability state which is made to usually stop the drive of an indicator from a movement state, and can carry out fixed time reception of the data signal from the data source. An automatic reset is usually carried out from the ready-for-receiving ability state after fixed time progress to a movement state, and time doubling is made unnecessary by forming the automatic reset circuit 53 which makes the rapid-traverse correction of the indicator which had stopped in the state of ready-for-receiving ability after an automatic reset, the same number is given to the same element as drawing 2 , and explanation is omitted. RS is a correction switch which is interlocked with

aforementioned RYUZU 24 and operates, and has a function as a terminal for a functional setup. 52 is a frequency divider which outputs 1Hz signal, the rapid-traverse signal S53, and the dividing signal S1 by considering the oscillation signal from an oscillator circuit 11 as an input. 51 is a mode store circuit, it inputs the one-shot signal S59 from the single-shot trigger circuit 50 which will operate if the aforementioned correction switch RS will be in ON state, carries out a change setup of the mode to the receive mode from the rapid-traverse mode which is a normal state, and outputs the receive mode signal S51. By inputting the receive mode signal S51, the control signal generating circuit 60 outputs the ready-for-receiving ability signal S2 and the detection enabling signal S3, and changes the indicator formula electronic clock 1 into a ready-for-receiving ability state.

[0026] 53 is an automatic reset circuit, and while the receive mode signal S51 is outputted from the aforementioned mode store circuit 51, it counts and memorizes the aforementioned 1Hz signal for creating indicator driving pulse PM. And the aforementioned 1Hz signal will output the automatic reset signal S54 which switches the aforementioned mode store circuit 51 to the rapid-traverse mode of a normal state, if the number-of-times input of predetermined is carried out. If the rapid-traverse mode signal S52 is outputted by switching the aforementioned mode store circuit 51, the aforementioned automatic reset circuit 53 will be counted until it is in agreement with 1Hz signal memorized by the rapid-traverse signal S53, and will output the pulse PF for a rapid-traverse drive simultaneously synchronizing with the rapid-traverse signal S53. 54 is an OR circuit, inputs the aforementioned pulse PM for an indicator drive, and the pulse PF for a rapid-traverse drive, and outputs the indicator driving signal S60.

[0027] Next, operation of the data transceiver system of the indicator formula electronic clock 1 equipped with the automatic reset circuit 53 which makes the rapid-traverse correction of the indicator in the above-mentioned composition is explained according to the timing diagram of drawing 6 . When the correction switch RS is in an OFF state, the converter drive circuit 14 inputs 1Hz signal from a frequency divider 52, and outputs the pulse for an indicator drive PM1. (Drawing 6 timing diagram t5) If aforementioned RYUZU 24 is pulled to one step next and the correction switch RS turns on, the receive mode signal S51 will be outputted from the mode store circuit 51. (Drawing 6 timing diagram t6) While the control signal generating circuit 60 outputs the ready-for-receiving ability signal S2 and the detection enabling signal S3 with this receive mode signal S51 and changing the indicator formula electronic clock 1 into a ready-for-receiving ability state, the automatic reset circuit 53 carries out the count start of the aforementioned 1Hz signal. The aforementioned automatic reset circuit 53

will output the automatic reset signal S54, if predetermined 1Hz (here 4 times) signal of number of times is counted, and the mode store circuit 51 is switched to rapid-traverse mode by this automatic reset signal S54, and it outputs the rapid-traverse mode signal S52. (Drawing 6 timing diagram t7) The automatic reset circuit 53 is counted until it is in agreement with the number of times (4 times) of 1Hz signal memorized by the aforementioned rapid-traverse signal S53 with the rapid-traverse mode signal S52, and it outputs the pulse PF for a rapid-traverse drive simultaneously synchronizing with the rapid-traverse signal S53. (Between t drawing 6 timing diagram t7-8) The pulse PF for a rapid-traverse drive passes OR circuit 54, serves as the indicator driving signal S60, and makes rapid-traverse correction.

[0028] Drawing 7 is the concrete circuitry view of the automatic reset circuit 53 in drawing 5 , and is constituted as follows. The 1st gate circuit which 53a permits passage of 1Hz signal, and 53b are the 2nd gate circuit which permits passage of the rapid-traverse signal S53. 53d is 1Hz signal store circuit, counts 1Hz signal which passed the aforementioned 1st gate circuit 53a, and outputs 1Hz signal storage information S58. 53c considers 1Hz signal storage information S58 as an input, and is a timer circuit by which 1Hz signal will output the automatic reset signal S54 to the aforementioned mode store circuit 51 if the number-of-times input of predetermined is carried out. It is a rapid-traverse driving-signal generating circuit, and 53f outputs the aforementioned PF for rapid-traverse driving pulses, whenever the rapid-traverse signal S52 which passed the aforementioned 2nd gate circuit 53b is inputted, it counts the rapid-traverse signal S52 simultaneously, and outputs the rapid-traverse information S57. 53e is a comparator circuit which inputs and compares 1Hz signal storage information S56 with the rapid-traverse information S57, if it is compared and is in agreement, it will output the coincidence signal S55, controls the aforementioned 2nd gate circuit 53b, and forbids passage of the rapid-traverse signal S52. Inputting 53g of coincidence signals S55 from aforementioned comparator-circuit 53e, it is the clear signal generating circuit which outputs the clear signal S56 of an one shot, and the aforementioned clear signal S56 initializes 53d of 1Hz signal store circuits, and 53f of rapid-traverse driving-signal generating circuits, and ends rapid-traverse correction.

[0029] Drawing 8 is the circuitry view of the converter drive circuit 14 in the indicator formula electronic clock 1 shown in drawing 2 of this invention. Tp1, Tp2, Tn1, and Tn2 are the MOS transistors for a drive, and they are controlled by motor driving pulse PM outputted from the aforementioned driving-signal generating circuit 13. DI1 and DI2 are diodes, carry out the clamp plastic surgery of the input signal which the aforementioned coil 15a for converters received, and output it to the aforementioned

detection permission circuit 17. Next, operation of the converter drive circuit 14 which has the above-mentioned composition is explained. Usually, when ON, or Tn1 and Tp2 are [Tp1 and Tn2 / OFF, Tp1, and Tn2] ON in the state of movement for OFF, Tn1, and Tp2, voltage is supplied in A points and B points of coil 15a for converters, and movement operation is performed. Moreover, in a normal state, Tp1 and Tp2 are [OFF, Tn1, and Tn2] ON, and Vss is impressed to A points of coil 15a for converters, and B points. If the ready-for-receiving ability signal S2 is inputted from the aforementioned control signal generating circuit 16 in this state, since ON, Tn2, Tp1, and Tp2 are turned off [them] by Tn1, A points fell to GND (Vss potential) and coil 15a for converters will be floated by B points, coil 15a for converters becomes the function of a receiver coil, and can receive the sending signal S28 from the aforementioned transmitter-receiver 2. Clamp plastic surgery is carried out for diodes DI1 and DI2, and the input signal generated in B points is sent to the aforementioned detection permission circuit 17.

[0030] In addition, although switched to the rapid-traverse mode of a normal state from the receive mode with the automatic reset signal S54 in this invention, it is possible to also make the operation to the OFF state of the correction switch RS from ON state perform return operation. Moreover, it is clear by not being limited to this, although the pulse PH for watch error measurement is set to 1Hz, and making high frequency of the pulse PH for watch error measurement that watch error adjustment time is shortened. Moreover, although the switch which is interlocked with RYUZU as a watch error measurement specification terminal, and operates is used, you may prepare an independent watch error measurement specification terminal. Moreover, although it is the method which supplies watch error adjustment data to a frequency divider, and performs watch error adjustment, it cannot be overemphasized that it is possible also in the method which controls the oscillation signal of an oscillator circuit to time sharing, and performs watch error adjustment. Although the watch error adjustment function was furthermore shown as an example, it is not limited to this and can apply to various setting up functions in an indicator formula electronic clock, such as a temperature control.

[0031]

[Effect of the Invention] Two-way communication stabilized without being interfered by the induced voltage of a stepping motor drive by stopping a clock by the above explanation according to this invention so that clearly, and performing two-way communication by making a timing signal into a synchronizing signal can be performed. Two-way communication is possible, without spoiling the function as a clock, since 1Hz

signal generated while having stopped the clock by the communicate mode furthermore is memorized and it is already correcting after a communicate mode end. A watch error regulating system with little memory space can be made possible by furthermore being adapted for watch error adjustment in this invention.

[Industrial Application] this invention relates to the data transceiver system of an indicator formula electronic clock.

[Description of the Prior Art] Although there is a watch error adjustment function as an example of the setting up function in an electronic clock conventionally, this watch error adjustment method has the thing in use which measures the period of the watch error signal outputted from an electronic clock, supplies the amount of watch error adjustments in digital one using an input terminal from the exterior by making a difference with a criteria period into the amount of watch error adjustments, and consists of non-volatile memory etc. and which a note of is made and the circuit is made to memorize. Moreover, the indicator formula electronic clock which receives an allowed-time signal from external allowed-time signal generation equipment as an example of a data receiving system which makes the coil for converters for an indicator drive serve a double purpose in an indicator formula electronic clock, and receives a signal, and performs watch error adjustment is proposed. (For example, JP,58-7190,B) In order that this clock may receive the allowed-time signal in a cycle of [from the outside] 1 second, it waits to set up a receiving state by operation of external actuator material, such as RYUZU, to change a frequency divider into a reset state simultaneously, and to input an allowed-time signal. If the allowed-time signal of the 1st shot is inputted, reset of a frequency divider will be canceled and a frequency deviation measuring circuit will start a count. And if the allowed-time signal of the 2nd shot is inputted after 1 second, while stopping a count, a frequency deviation store circuit is made to memorize the frequency deviation which the aforementioned frequency deviation measuring circuit counted, and automatic watch error adjustment is ended. And reset is applied again, reset is automatically canceled after fixed time, and normal operation is started. namely, the allowed-time signal in a cycle of [which is supplied from the outside in the above-mentioned operation / exact] 1 second -- an internal counter -- counting -- carrying out -- the enumerated data -- as the period of 1 future second -- a time check -- it is the one-sided receiving method which operates, and the coil for converters is used for reception of the allowed-time signal

[Effect of the Invention] Two-way communication stabilized without being interfered by the induced voltage of a stepping motor drive by stopping a clock by the above explanation according to this invention so that clearly, and performing two-way

communication by making a timing signal into a synchronizing signal can be performed. Two-way communication is possible, without spoiling the function as a clock, since 1Hz signal generated while having stopped the clock by the communicate mode furthermore is memorized and it is already correcting after a communicate mode end. A watch error regulating system with little memory space can be made possible by furthermore being adapted for watch error adjustment in this invention.

[Effect of the Invention] Two-way communication stabilized without being interfered by the induced voltage of a stepping motor drive by stopping a clock by the above explanation according to this invention so that clearly, and performing two-way communication by making a timing signal into a synchronizing signal can be performed. Two-way communication is possible, without spoiling the function as a clock, since 1Hz signal generated while having stopped the clock by the communicate mode furthermore is memorized and it is already correcting after a communicate mode end. A watch error regulating system with little memory space can be made possible by furthermore being adapted for watch error adjustment in this invention.

[Means for Solving the Problem] In order to make the above-mentioned purpose attain, this invention is considered as the following composition. In the data transceiver system of the electronic clock which consists of the data source which generates a data signal, and an electronic clock which makes the coil for converters for an indicator drive serve a double purpose, and receives the data signal from the aforementioned data source A timing signal generating means to generate a timing signal in the aforementioned electronic clock, The driving-signal generating circuit which generates an indicator driving pulse, and a converter drive circuit, The electronic switch for changing the aforementioned timing signal generating means and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting, It is characterized by having a terminal for a functional setup for controlling this electronic switch, making the coil for converters serve a double purpose, while controlling the aforementioned electronic switch by the aforementioned terminal for a functional setup and having set up function mode with it, and performing transceiver operation by making the aforementioned timing signal into a synchronizing signal.

[0005] Furthermore, the time return circuit which memorizes the indicator driving pulse generated while the aforementioned electronic switch has set up function mode is prepared, and it is characterized by the aforementioned electronic switch making rapid-traverse correction for an indicator according to the information on the aforementioned time return circuit at the time of a time mode return.

[0006] Furthermore, it is characterized by establishing a timer means to set up function

mode, for the aforementioned time return circuit operating by the terminate signal of this timer means of operation, and the aforementioned time return circuit making rapid-traverse correction for an indicator.

[0007] Furthermore, an oscillator circuit and a watch error adjustment means to adjust the frequency of the output signal of this oscillator circuit, A watch error adjustment data-storage means to memorize the watch error adjustment data of this watch error adjustment means, The driving-signal generating circuit which generates an indicator driving pulse, and a converter drive circuit, The indicator formula electronic clock equipped with the coil for converters driven by the output signal of this converter drive circuit, Detect a signal and watch error measurement is performed. the criteria which have the periodicity generated from the coil for converters of this indicator formula electronic clock -- electromagnetism -- It is the watch error regulating system constituted by the watch error adjusting device which makes a signal and is outputted to the aforementioned indicator formula electronic clock. the measurement result -- the watch error adjustment data of an indicator formula electronic clock -- creating -- the watch error adjustment data -- adjustment -- electromagnetism -- The watch error signal generating circuit in which the aforementioned indicator formula electronic clock generates the pulse for watch error measurement, Having had the watch error measurement specification terminal for controlling the electronic switch and this electronic switch for changing this watch error signal generating circuit and the aforementioned driving-signal generating circuit to the aforementioned converter drive circuit, and connecting is characterized by things.

[Example] The example which was adapted for the watch error adjustment function in the transceiver system of this invention with the drawing below is explained. Drawing 1 is the block diagram of the watch error regulating system of the indicator formula electronic clock equipped with the watch error adjustment function which shows the first example in this invention. 1 is the indicator formula electronic clock equipped with the correction switch RS which is interlocked with RYUZU 24 for stopping coil 15a for converters for driving an indicator, and an indicator drive, and correcting time, and operates. 2 is a watch error adjusting device and is equipped with the coil 31 for transmission and reception. The aforementioned coil 31 for transmission and reception transmits and receives between the aforementioned coil 15a for converters. the criteria which the aforementioned watch error adjusting device 2 generates from coil 15for converters a at the time of time correction of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- a signal S40 -- the aforementioned coil 31 for transmission and reception -- receiving -- watch error measurement -- carrying out --

the measurement result -- the watch error adjustment data of an indicator formula electronic clock 1 -- creating -- the aforementioned criteria -- electromagnetism -- a signal S40 -- synchronizing -- the aforementioned watch error adjustment data -- adjustment -- electromagnetism -- it considers as a signal 41 and it transmits

[0009] Drawing 2 is the circuit block diagram of the indicator formula electronic clock 1 in this invention. 11 is an oscillator circuit which makes a quartz resonator a reference signal, and 12 is a frequency divider which outputs 1Hz signal and the dividing signal S1 for creating an indicator driving pulse by considering the oscillation signal from an oscillator circuit 11 as an input. 13 is a driving-signal generating circuit and outputs the pulse PM for an indicator drive to the converter drive circuit 14 as a signal which considers 1Hz signal from a frequency divider 12 as an input, and drives a motor. 15a has the function as a coil for transmission and reception to be the coil for converters with which the converter 15 for driving the indicator driving gear 23 was equipped, and to perform transmission and reception with the aforementioned watch error adjusting device 2. 24 is RYUZU for correcting the time of the indicator driving gear 23, and is in zero step of position in a normal state. By lengthening one step of RYUZU 24, Switch RS is a correction switch which interlocks and operates, has a function as a watch error measurement specification terminal, and forbids the pulse PM output for an indicator drive from the driving-signal generating circuit 13. 25 is a watch error signal generating circuit, considers 1Hz signal from a frequency divider 12 as an input, and outputs the pulse PH for watch error measurement of the pulse width which is the grade which is a period of 1 second and a stepping motor does not drive to the converter drive circuit 14.

[0010] 26 is an electronic switch which considers the pulse PM for an indicator drive, and the pulse PH for watch error measurement as an input, chooses the pulse PM for an indicator drive in a normal state, chooses the pulse PH for watch error measurement in the state of the correction which lengthened one step of RYUZU 24, and is outputted to the converter drive circuit 14. The pulse PH for watch error measurement outputted from the watch error signal generating circuit 25 in this example serves as a timing signal transmitted to the aforementioned watch error adjusting device 2, therefore the watch error signal generating circuit 25 has a function as a timing signal generating circuit. if, as for the aforementioned coil 15a for converters, the pulse PH for watch error measurement is supplied -- criteria -- electromagnetism -- a signal S40 is generated 16 is a control signal generating circuit, inputs the aforementioned dividing signal S1, and outputs many control signals of the ready-for-receiving ability signal S2 grade which changes the aforementioned converter drive circuit 14 into a receiving state. the detection enabling signal S3 which 17 is a detection permission circuit and is outputted

from the aforementioned control signal generating circuit 16 -- adjustment -- electromagnetism -- passage of the input signal S12 from coil 15for converters a which received the signal S41 is forbidden or permitted 18 is a watch error adjustment signal-detection circuit, and changes into the watch error adjustment signal S4 the input signal S12 which passed through the aforementioned detection permission circuit 17. 19 is a shift register, memorizes the watch error adjustment signal S4 from the watch error adjustment signal-detection circuit 18 with the data shift signal S5 outputted from the aforementioned control signal generating circuit 16, and outputs a data signal D1 and a data signal D2.

[0011] It judges whether the data signal D1 of 20 memorized with the aforementioned shift register 19 by the data judging signal S6 which is a rewriting judging circuit and is outputted from the aforementioned control signal generating circuit 16 is effective, and if right, the data rewriting enabling signal S7 will be outputted to the aforementioned control signal generating circuit 16. 21 is a booster circuit, the elimination signal S8 and write-in signal S9 which are outputted from the aforementioned control signal generating circuit 16 perform pressure-up operation, and only fixed time outputs the pressure-up signal S10. 22 is the amount store circuit of watch error adjustments which consists of non-volatile memory etc., and when the data signal D2 from the aforementioned shift register 19 and the pressure-up signal S10 from a booster circuit 21 are considered as an input and elimination of data and writing are performed by the elimination signal S8 and write-in signal S9 which are outputted from the aforementioned control signal generating circuit 16, it supplies the watch error data D3 to the aforementioned frequency divider 12.

[0012] the watch error adjusting device [in / this example / a view 3 is a circuit block diagram of the watch error adjusting device 2 in this invention, and] 2 -- the criteria from the aforementioned indicator formula electronic clock 1 -- electromagnetism -- the watch error adjustment data which receive a signal S40 as a watch error detecting signal, perform watch error measurement based on this, and follow the result -- adjustment -- electromagnetism -- it is the watch error adjusting device transmitted as a signal 41 31 is the aforementioned coil for transmission and reception. the change signal S21 from the transceiver control circuit 39 which 32 is a transceiver electronic switch and is mentioned later -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- receiving a signal S40 **** -- coil 15a for converters -- adjustment -- electromagnetism -- change control of transmitting a signal 41 is carried out 33 -- a gate circuit -- it is -- the aforementioned criteria -- electromagnetism -- passage of a signal S40 is forbidden or permitted 34 is a watch error signal-detection circuit, and

consists of filter circuit 34a and amplifying-circuit 34b -- having -- the criteria from the aforementioned gate circuit 33 -- electromagnetism -- a signal S40 is inputted and it detects as a watch error detection pulse PT 35 is a period-measurement circuit, considers the aforementioned watch error detection pulse PT as an input, measures the interval of two or more watch error detection pulses PT with the reference signal S13 from the reference signal generating circuit 36, and outputs measurement data D4.

[0013] at the same time it outputs the system clear signal S22 which 37 is a measurement start store circuit and initializes the watch error adjusting device 2 by operation of a switch 38 -- the receiving enabling signal S23 -- outputting -- the aforementioned gate circuit 33 -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- it is controlling to permit passage of a signal S40 39 is a transceiver control circuit and outputs many control signals of the change signal S21 grade which considers the aforementioned watch error detection pulse PT as an input, and makes the aforementioned transceiver electronic switch 32 a send state. 47 is the 1st data-storage circuit, it considers measurement data D4 from the aforementioned period-measurement circuit 35 as an input, memorizes the aforementioned measurement data D4 with the periodic latch signal S31 outputted whenever the aforementioned transceiver control circuit 39 inputs the aforementioned watch error detection pulse PT, and outputs the periodic stored data D8. 48 is the 2nd data-storage circuit, newly memorizes the aforementioned periodic stored data D8 with the NG signal S34 outputted from the comparison-test circuit 49 which considers the periodic stored data D8 from the aforementioned 1st data-storage circuit 47 as an input, and mentions it later, and outputs it as periodic criteria data D9. the value which 49 is a comparison-test circuit, considered the aforementioned periodic stored data D8 and the aforementioned periodic criteria data D9 as an input, and carried out the comparison test of the aforementioned periodic stored data D8 and the aforementioned periodic criteria data D9 with the comparison signal S32 outputted from the aforementioned transceiver control circuit 39, outputted an O.K. signal S33 to the aforementioned transceiver control circuit 39, and compared it when the value which compared was specification within the limits -- specification -- if out of range, an NG signal S34 will output to the

[0014] 41 is the amount arithmetic circuit of watch error adjustments, and the operation of the amount of watch error adjustments is started by the operation instruction signal S24 which inputs the aforementioned periodic stored data D8, and is outputted from the aforementioned transceiver control circuit 39. After an operation is completed, while outputting the amount data D5 of adjustments, the operation terminate signal S25 is

outputted to the aforementioned transceiver control circuit 39. 42 is a transmit data creation circuit, inputs the amount data D5 of adjustments from the aforementioned amount arithmetic circuit 41 of watch error adjustments, and changes them into the data signal D6 of binary code form. 43 is a rewriting command creation circuit and creates the data signal D7 of the meaning of transmitting a data signal D6 after this, to the indicator formula electronic clock 1. 45 is a display circuit, considers the amount data D5 of adjustments from the aforementioned amount arithmetic circuit 41 of watch error adjustments as an input, and consists of a conversion circuit changed into ppm or sunlight to a reference value, and a drive circuit which drives the display 46 equipped with LCD etc. It is a number-of-times counting circuit of NG, 50 inputs the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and if it counts and becomes more than the number of times with a fixed count (for example, 5 times), it will output a reset signal S35. This reset signal S35 clears and initializes the aforementioned measurement start store circuit 37 and a display circuit 45.

[0015] 44 is a data sending circuit and outputs the sending signal S28 which serial-data-ized the aforementioned data signal D7 and the data signal D6 by the clock signal S27 which is latched with the latch signal S26 which considers the aforementioned data signal D6 and a data signal D7 as an input, and is outputted from the aforementioned transceiver control circuit 39, and is outputted from the clock generation circuit 40 mentioned later. this sending signal S28 -- the aforementioned coil 31 for transmission and reception -- adjustment -- electromagnetism -- it is transmitted to the aforementioned indicator formula electronic clock 1 as a signal S41 40 is a clock generation circuit and outputs the clock signal S27 which drives the aforementioned data sending circuit 44 by the seizure signal S29 outputted from the aforementioned transceiver control circuit 39. moreover -- at the same time the transmitting terminate signal S30 outputted from the aforementioned transceiver control circuit 39 resets the aforementioned measurement start store circuit 37 and it initializes the watch error adjusting device 2 -- the aforementioned gate circuit 33 -- the criteria from aforementioned coil 15for converters a -- electromagnetism -- passage of a signal S40 is forbidden

[0016] Next, operation of the watch error regulating system of the indicator formula electronic clock 1 equipped with the watch error adjustment function in the above-mentioned composition is explained according to the timing diagram of drawing 4 . The normal operation of the aforementioned indicator formula electronic clock 1 has RYUZU 24 in zero step of position, and the aforementioned change circuit 26 chooses and outputs motor driving pulse PM. By outputting the converter driving signal S11

and supplying coil 15a for converters, converter coil 15a drives the indicator driving gear 23, and the converter drive circuit 14 which inputs this motor driving pulse PM performs a time stamp by movement for 1 second. In the state of correction, 1 stage length of RYUZU 24 is carried out, the correction switch RS with which RYUZU 24 is interlocked with and it operates will be in ON state, and a correcting signal S14 will be outputted. Forbidding the pulse PM output for an indicator drive from the aforementioned driving-signal generating circuit 13 by this correcting signal S14, the aforementioned change circuit 26 chooses and outputs the pulse PH for watch error measurement simultaneously. supplying this pulse PH for watch error measurement to coil 15a for converters -- coil 15a for converters -- criteria -- electromagnetism -- a signal S40 occurs the aforementioned control signal generating circuit 16 inputting the dividing signal S1 from the back frequency divider 12 with which the pulse PH for watch error measurement was outputted, and outputting the ready-for-receiving ability signal S2 -- the adjustment from the watch error adjusting device 2 -- electromagnetism -- the converter drive circuit 14 is changed to a receiving state so that a signal S41 can be received by coil 15a for converters Simultaneously, the aforementioned control signal generating circuit 16 outputs the detection enabling signal S3, and permits passage of an input signal S12 to the detection permission circuit 17. this -- the indicator formula electronic clock 1 -- the first pulse PH for watch error measurement -- criteria -- electromagnetism -- after outputting as a signal S40, only the time of the ready-for-receiving ability signal S2 is held in the ready-for-receiving ability state before the following pulse PH output for watch error measurement

[0017] on the other hand -- the watch error adjusting device 2 -- the criteria of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- in order to receive a signal S40, it initializes by operation of a switch 38 first The aforementioned measurement start store circuit 37 outputs the system clear signal S22 and the receiving enabling signal S23 by operation of this switch 38. with the system clear signal S22, the transceiver electronic switch 32 changes the receive mode -- having -- the criteria from the aforementioned indicator formula electronic clock 1 -- electromagnetism -- it changes into the receiving state where a signal S40 is receivable Simultaneously, the aforementioned rewriting command creation circuit 43 creates and outputs a data signal D7 with the system clear signal S22. The aforementioned period-measurement circuit 35, the aforementioned 2nd data-storage circuit 48, and the number-of-times counting circuit 50 of NG are cleared simultaneously. further -- the receiving enabling signal S23 from the aforementioned measurement start store circuit 37 -- a gate circuit 33 -- controlling -- the criteria from the aforementioned coil 31 for

transmission and reception -- electromagnetism -- passage of a signal S40 is permitted this state -- the criteria of the aforementioned indicator formula electronic clock 1 -- electromagnetism -- if a signal S40 is received, an input signal will pass a gate circuit 33 and will input it into the watch error signal-detection circuit 34 -- having -- this watch error signal-detection circuit 34 -- the first criteria -- electromagnetism -- the watch error detection pulse PT which is a signal S40 is detected (Timing of the drawing 4 timing diagram t1)

[0018] The period-measurement circuit 35 ends the count of the reference signal S13 from the reference signal generating circuit 36 counted by t1 until now the time of the first watch error detection pulse PT 1 being inputted, outputs it as measurement data D4 (the first value is not right), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 1 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage circuit 47 memorizes the measurement data D4 at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8. Next, the aforementioned transceiver control circuit 39 outputs the comparison signal S32. With this comparison signal S32, the aforementioned comparison-test circuit 49 compares the aforementioned periodic stored data D8 with the aforementioned periodic criteria data D9 (the first value is 0) outputted from the 2nd data-storage circuit 48, and the NG signal S34 is outputted. The 2nd data-storage circuit 48 memorizes the aforementioned periodic stored data D8 as new periodic criteria data D9 with this NG signal S34. . Simultaneously, the aforementioned number-of-times counting circuit 50 of NG counts the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and the number of times of a count is set to 1.

[0019] next, the criteria of the indicator formula electronic clock 1 to a degree -- electromagnetism -- a signal S40 outputs -- having -- these criteria -- electromagnetism -- the 2nd watch error detection pulse PT 2 outputs from the aforementioned watch error signal-detection circuit 34 by receiving a signal S40 with the aforementioned coil 31 for transmission and reception -- having (timing of the drawing 4 timing diagram t2) -- The period-measurement circuit 35 ends the count of the reference signal S13 counted from t1 the time of the first watch error detection pulse PT 1 being inputted, outputs it as measurement data D4 (period T1 of the drawing 4 timing diagrams t1 and t2), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 2 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage

circuit 47 memorizes the measurement data D4 (T1) at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8 (T1). Next, the aforementioned transceiver control circuit 39 compares the aforementioned periodic criteria data D9 to which the comparison signal S32 is outputted and the aforementioned comparison-test circuit 49 is outputted by this comparison signal S32 from the aforementioned periodic stored data D8 and the 2nd data-storage circuit 48, and outputs the NG signal S34. With this NG signal S34, the 2nd data-storage circuit 48 memorizes the aforementioned periodic stored data D8 as new periodic criteria data D9 (T1), simultaneously, the aforementioned number-of-times counting circuit 50 of NG counts the NG signal S34 outputted from the aforementioned comparison-test circuit 49, and the number of times of a count is set to 2.

[0020] further -- the criteria from the indicator formula electronic clock 1 -- electromagnetism -- a signal S40 outputs -- having -- these criteria -- electromagnetism -- the 3rd watch error detection pulse PT 3 outputs from the aforementioned watch error signal-detection circuit 34 by receiving a signal S40 with the aforementioned coil 31 for transmission and reception -- having (timing of the drawing 4 timing diagram t3) -- The period-measurement circuit 35 ends the count of the reference signal S13 counted from t2 the time of the watch error detection pulse PT 2 being inputted, outputs it as measurement data D4 (period T2 of the drawing 4 timing diagrams t2 and t3), and starts a count again. Simultaneously, the aforementioned transceiver control circuit 39 will output the periodic latch signal S31, if the watch error detection pulse PT 3 is inputted. With this periodic latch signal S31, the aforementioned 1st data-storage circuit 47 memorizes the measurement data D4 (T2) at the time of the aforementioned period-measurement circuit 35 ending a count, and outputs the periodic stored data D8 (T2). Next, since the value which compared and compared the aforementioned periodic criteria data D9 (T1) to which the aforementioned transceiver control circuit 39 outputs the comparison signal S32, and the aforementioned comparison-test circuit 49 is outputted by this comparison signal S32 from the aforementioned periodic stored data D8 (T2) and the 2nd data-storage circuit 48 is specification within the limits, the O.K. signal S33 is outputted to the aforementioned transceiver control circuit 39, and the aforementioned transceiver control circuit 39 outputs the operation-instruction signal S24.

[0021] If this operation instruction signal S24 is outputted to the amount arithmetic circuit 41 of watch error adjustments, the amount arithmetic circuit 41 of watch error adjustments will start the operation of the amount of watch error adjustments from the aforementioned periodic stored data D8 (T2), and after an operation is completed, while

outputting the amount data D5 of adjustments which are the result of an operation, the operation terminate signal S25 is outputted to the aforementioned transceiver control circuit 39. The amount data D5 of adjustments outputted from the aforementioned amount arithmetic circuit 41 of watch error adjustments are changed into the data signal D6 of binary code form in the transmit data creation circuit 42. Moreover, the amount data D5 of adjustments are simultaneously changed into sunlight by the display circuit 45, and the value is displayed on display 46. If the aforementioned operation terminate signal S25 is outputted to the aforementioned transceiver control circuit 39, the transceiver control circuit 39 will output the latch signal S26, and will memorize the aforementioned data signal D7 and a data signal D6 to the data sending circuit 44. Moreover, the change signal S21 is outputted synchronizing with the aforementioned watch error detection pulse PT 3 (drawing 4 timing diagram t4), and the transceiver electronic switch 32 is set as a send state. And by the clock signal S27 from the clock generation circuit 40 which operates by the seizure signal S29 outputted to a degree from the transceiver control circuit 39, the data signal D7 and data signal D6 which are memorized by the data sending circuit 44 are outputted one by one as a sending signal S28. A sending signal S28 is transmitted to the aforementioned indicator formula electronic clock 1 as an adjustment signal S41 through the transceiver electronic switch 32 and the coil 31 for transmission and reception. If it finishes transmitting a sending signal S28 altogether, the transceiver control circuit 39 will output the transmitting terminate signal S30.

[0022] The timing to which a series of aforementioned sending signals S28 are transmitted suits the state, i.e., the receiving state of the indicator formula electronic clock 1, where the control signal generating circuit 16 of the indicator formula electronic clock 1 is outputting the ready-for-receiving ability signal S2 as shown in the change signal S21 of the timing diagram of drawing 4 , and the ready-for-receiving ability signal S2 of the aforementioned indicator formula electronic clock 1. The transmitting terminate signal S30 from the aforementioned transceiver control circuit 39 is inputted into the aforementioned measurement start store circuit 37, and the receiving enabling signal S23 stops and it has the aforementioned gate circuit 33 closed by resetting this measurement start store circuit 37. One watch error adjustment operation is completed above, and it is resumed by pushing a switch 38 to perform watch error adjustment operation again.

[0023] The adjustment MAG signal S41 transmitted from the aforementioned watch error adjusting device 2 on the other hand explains the operation below, although received by coil 15a for converters of the indicator formula electronic clock 1. The

aforementioned indicator formula electronic clock 1 is the ready-for-receiving ability signal S2 which the control signal generating circuit 16 outputs, changes the converter drive circuit 14 to a receiving state, and receives the adjustment MAG signal S41 which consisted of a data signal D7 transmitted from the watch error adjusting device 2, and a data signal D6 as an input signal S12 by coil 15a for converters. The input signal S12 which received is detected through the detection permission circuit 17 in the watch error adjustment signal-detection circuit 18, and is outputted as watch error adjustment signal S4. After a shift register 19 memorizes one by one by the data shift signal S5 which the control signal generating circuit 16 outputs and all storage of watch error adjustment signal S4 is completed, detected watch error adjustment signal S4 makes the aforementioned data signal D7 a data signal D1, is outputted to the aforementioned rewriting judging circuit 20, and outputs to the aforementioned watch error adjustment store circuit 22 by making the aforementioned data signal D6 into a data signal D2. The control signal generating circuit 16 will output the data judging signal S6 to the aforementioned rewriting judging circuit 20, if it finishes outputting the data shift signal S5, and it judges whether it is effective, and if the data signal D1 is effective, as for this rewriting judging circuit 20, it will output the data rewriting enabling signal S7. However, when the judgment result in the aforementioned rewriting judging circuit 20 is invalid, the data rewriting enabling signal S7 is not outputted, and watch error adjustment is not performed.

[0024] The control signal generating circuit 16 will output the elimination signal S8, if the data rewriting enabling signal S7 is inputted, it sets the amount store circuit 22 of watch error adjustments as elimination mode, operates a booster circuit S21 simultaneously, and eliminates the data of the amount store circuit 22 of watch error adjustments with the pressure-up signal S10. Then, the control signal generating circuit 16 outputs write-in signal S9, and watch error adjustment ends it by setting the amount store circuit 22 of watch error adjustments as write-in mode, operating a booster circuit 21 simultaneously, and writing the data signal D2 which is the amount data of adjustments in the amount store circuit 22 of watch error adjustments with the pressure-up signal S10.

[0025] Drawing 5 is the circuit block diagram of the indicator formula electronic clock 1 of the second example in this invention. this example sets up the ready-for-receiving ability state which is made to usually stop the drive of an indicator from a movement state, and can carry out fixed time reception of the data signal from the data source. An automatic reset is usually carried out from the ready-for-receiving ability state after fixed time progress to a movement state, and time doubling is made unnecessary by

forming the automatic reset circuit 53 which makes the rapid-traverse correction of the indicator which had stopped in the state of ready-for-receiving ability after an automatic reset, the same number is given to the same element as drawing 2 , and explanation is omitted. RS is a correction switch which is interlocked with aforementioned RYUZU 24 and operates, and has a function as a terminal for a functional setup. 52 is a frequency divider which outputs 1Hz signal, the rapid-traverse signal S53, and the dividing signal S1 by considering the oscillation signal from an oscillator circuit 11 as an input. 51 is a mode store circuit, it inputs the one-shot signal S59 from the single-shot trigger circuit 50 which will operate if the aforementioned correction switch RS will be in ON state, carries out a change setup of the mode to the receive mode from the rapid-traverse mode which is a normal state, and outputs the receive mode signal S51. By inputting the receive mode signal S51, the control signal generating circuit 60 outputs the ready-for-receiving ability signal S2 and the detection enabling signal S3, and changes the indicator formula electronic clock 1 into a ready-for-receiving ability state.

[0026] 53 is an automatic reset circuit, and while the receive mode signal S51 is outputted from the aforementioned mode store circuit 51, it counts and memorizes the aforementioned 1Hz signal for creating indicator driving pulse PM. And the aforementioned 1Hz signal will output the automatic reset signal S54 which switches the aforementioned mode store circuit 51 to the rapid-traverse mode of a normal state, if the number-of-times input of predetermined is carried out. If the rapid-traverse mode signal S52 is outputted by switching the aforementioned mode store circuit 51, the aforementioned automatic reset circuit 53 will be counted until it is in agreement with 1Hz signal memorized by the rapid-traverse signal S53, and will output the pulse PF for a rapid-traverse drive simultaneously synchronizing with the rapid-traverse signal S53. 54 is an OR circuit, inputs the aforementioned pulse PM for an indicator drive, and the pulse PF for a rapid-traverse drive, and outputs the indicator driving signal S60.

[0027] Next, operation of the data transceiver system of the indicator formula electronic clock 1 equipped with the automatic reset circuit 53 which makes the rapid-traverse correction of the indicator in the above-mentioned composition is explained according to the timing diagram of drawing 6 . When the correction switch RS is in an OFF state, the converter drive circuit 14 inputs 1Hz signal from a frequency divider 52, and outputs the pulse for an indicator drive PM1. (Drawing 6 timing diagram t5) If aforementioned RYUZU 24 is pulled to one step next and the correction switch RS turns on, the receive mode signal S51 will be outputted from the mode store circuit 51. (Drawing 6 timing diagram t6) While the control signal generating circuit 60 outputs the

ready-for-receiving ability signal S2 and the detection enabling signal S3 with this receive mode signal S51 and changing the indicator formula electronic clock 1 into a ready-for-receiving ability state, the automatic reset circuit 53 carries out the count start of the aforementioned 1Hz signal. The aforementioned automatic reset circuit 53 will output the automatic reset signal S54, if predetermined 1Hz (here 4 times) signal of number of times is counted, and the mode store circuit 51 is switched to rapid-traverse mode by this automatic reset signal S54, and it outputs the rapid-traverse mode signal S52. (Drawing 6 timing diagram t7) The automatic reset circuit 53 is counted until it is in agreement with the number of times (4 times) of 1Hz signal memorized by the aforementioned rapid-traverse signal S53 with the rapid-traverse mode signal S52, and it outputs the pulse PF for a rapid-traverse drive simultaneously synchronizing with the rapid-traverse signal S53. (Between t drawing 6 timing diagram t7-8) The pulse PF for a rapid-traverse drive passes OR circuit 54, serves as the indicator driving signal S60, and makes rapid-traverse correction.

[0028] Drawing 7 is the concrete circuitry view of the automatic reset circuit 53 in drawing 5 , and is constituted as follows. The 1st gate circuit which 53a permits passage of 1Hz signal, and 53b are the 2nd gate circuit which permits passage of the rapid-traverse signal S53. 53d is 1Hz signal store circuit, counts 1Hz signal which passed the aforementioned 1st gate circuit 53a, and outputs 1Hz signal storage information S58. 53c considers 1Hz signal storage information S58 as an input, and is a timer circuit by which 1Hz signal will output the automatic reset signal S54 to the aforementioned mode store circuit 51 if the number-of-times input of predetermined is carried out. It is a rapid-traverse driving-signal generating circuit, and 53f outputs the aforementioned PF for rapid-traverse driving pulses, whenever the rapid-traverse signal S52 which passed the aforementioned 2nd gate circuit 53b is inputted, it counts the rapid-traverse signal S52 simultaneously, and outputs the rapid-traverse information S57. 53e is a comparator circuit which inputs and compares 1Hz signal storage information S56 with the rapid-traverse information S57, if it is compared and is in agreement, it will output the coincidence signal S55, controls the aforementioned 2nd gate circuit 53b, and forbids passage of the rapid-traverse signal S52. Inputting 53g of coincidence signals S55 from aforementioned comparator-circuit 53e, it is the clear signal generating circuit which outputs the clear signal S56 of an one shot, and the aforementioned clear signal S56 initializes 53d of 1Hz signal store circuits, and 53f of rapid-traverse driving-signal generating circuits, and ends rapid-traverse correction.

[0029] Drawing 8 is the circuitry view of the converter drive circuit 14 in the indicator formula electronic clock 1 shown in drawing 2 of this invention. Tp1, Tp2, Tn1, and Tn2

are the MOS transistors for a drive, and they are controlled by motor driving pulse PM outputted from the aforementioned driving-signal generating circuit 13. DI1 and DI2 are diodes, carry out the clamp plastic surgery of the input signal which the aforementioned coil 15a for converters received, and output it to the aforementioned detection permission circuit 17. Next, operation of the converter drive circuit 14 which has the above-mentioned composition is explained. Usually, when ON, or Tn1 and Tp2 are [Tp1 and Tn2 / OFF, Tp1, and Tn2] ON in the state of movement for OFF, Tn1, and Tp2, voltage is supplied between A points and B point of coil 15a for converters, and movement operation is performed. Moreover, in a normal state, Tp1 and Tp2 are [OFF, Tn1, and Tn2] ON, and Vss is impressed to A points of coil 15a for converters, and the B point. If the ready-for-receiving ability signal S2 is inputted from the aforementioned control signal generating circuit 16 in this state, since ON, Tn2, Tp1, and Tp2 are turned off [them] by Tn1, A points fell to GND (Vss potential) and coil 15a for converters will be floated by the B point, coil 15a for converters becomes the function of a receiver coil, and can receive the sending signal S28 from the aforementioned transmitter-receiver 2. Clamp plastic surgery is carried out for diodes DI1 and DI2, and the input signal generated in the B point is sent to the aforementioned detection permission circuit 17.

[0030] In addition, although switched to the rapid-traverse mode of a normal state from the receive mode with the automatic reset signal S54 in this invention, it is possible to also make the operation to the OFF state of the correction switch RS from ON state perform return operation. Moreover, it is clear by not being limited to this, although the pulse PH for watch error measurement is set to 1Hz, and making high frequency of the pulse PH for watch error measurement that watch error adjustment time is shortened. Moreover, although the switch which is interlocked with RYUZU as a watch error measurement specification terminal, and operates is used, you may prepare an independent watch error measurement specification terminal. Moreover, although it is the method which supplies watch error adjustment data to a frequency divider, and performs watch error adjustment, it cannot be overemphasized that it is possible also in the method which controls the oscillation signal of an oscillator circuit to time sharing, and performs watch error adjustment. Although the watch error adjustment function was furthermore shown as an example, it is not limited to this and can apply to various setting up functions in an indicator formula electronic clock, such as a temperature control.

[Brief Description of the Drawings]

[Drawing 1] It is the block diagram of the watch error regulating system by an indicator

formula electronic clock and a watch error adjusting device equipped with the watch error adjustment function which shows the first example of this invention.

[Drawing 2] It is the block diagram of the indicator formula clock of drawing 1 .

[Drawing 3] It is the block diagram of the watch error adjusting device of drawing 1 .

[Drawing 4] It is the timing diagram view showing operation of the first example of this invention.

[Drawing 5] It is the block diagram of the indicator formula electronic clock in the second example of this invention.

[Drawing 6] It is the timing diagram view showing operation of the second example of this invention.

[Drawing 7] It is the circuitry view of the automatic reset circuit 53 in drawing 6 .

[Drawing 8] It is the circuitry view of the converter drive circuit 14 in drawing 1 .

[Description of Notations]

1 ... Indicator Formula Electronic Clock

2 ... Watch Error Adjusting Device

13 ... Driving-Signal Generating Circuit

16 ... Control Signal Generating Circuit

15a ... Coil for converters

18 ... Watch Error Adjustment Signal-Detection Circuit

20 ... Rewriting Judging Circuit

22 ... The Amount Store Circuit of Watch Error Adjustments

25 ... Watch Error Signal Generating Circuit

26 ... Change Circuit

31 ... Coil for Transmission and Reception

32 ... Transceiver Electronic Switch

34 ... Watch Error Signal-Detection Circuit

39 ... Transceiver Control Circuit

44 ... Data Sending Circuit

51 ... Mode Store Circuit

53 ... Automatic Reset Circuit

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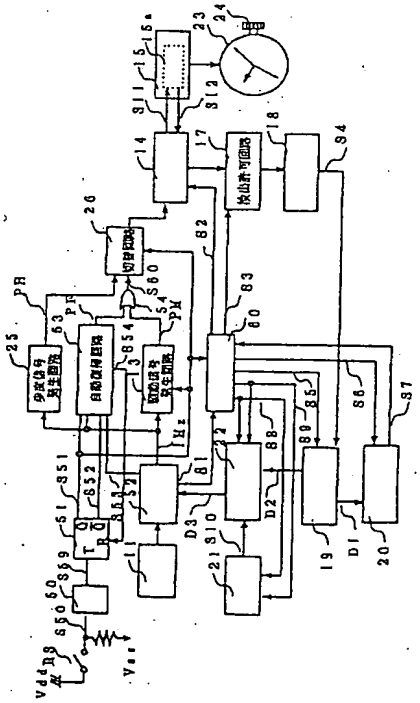
(54)【発明の名称】　指針式電子時計のデータ送受信システム

(57)【要約】

【目的】　本発明は指針式電子時計のデータ送受信システムに関するものである。

【構成】　歩度信号発生回路２５と駆動信号発生回路１３との出力信号を変換機用コイル１５ａに切替え供給するための切替回路２６を設け通信機能モード時に歩度信号発生回路のタイミング信号を変換機用コイル１５ａに供給して双方向通信を行ない、かつモード指定時における１Ｈｚ信号を記憶してモード終了時に時刻の自動復帰を行なう。

【効果】　時計を止めてかつタイミング信号を同期信号として双方向通信を行なうことによってパルスモータ駆動の誘起電圧に邪魔されることなく安定した双方向通信を行なうことができる。さらに通信モードで時計を止めている間に発生する１Ｈｚ信号を記憶し通信モード終了後早修正しているため時計としての機能を損ねることなく双方向通信ができる。



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【特許請求の範囲】

【請求項１】　データ信号を発生するデータ送信装置と、指針駆動用の変換機用コイルを兼用して前記データ送信装置からのデータ信号を受信する電子時計より構成される電子時計のデータ受信システムに於て、前記電子時計にはタイミング信号を発生する歩度信号発生手段と、指針駆動パルスを発生する駆動信号発生回路と、変換機駆動回路と、前記タイミング信号発生手段と前記駆動信号発生回路とを前記変換機駆動回路に対して切り替え接続するための切替回路と、該切替回路を制御するための機能設定用端子とを備え前記機能設定用端子によって前記切替回路を制御して機能モードを設定している間前記変換機用コイルを兼用し、かつ前記タイミング信号を同期信号として送受信動作を行うことを特徴とする指針式電子時計のデータ送受信システム。

【請求項２】　前記切替回路が機能モードを設定している間に発生する指針駆動パルスを記憶する時刻復帰回路を設け、前記切替回路が時刻モード復帰時に前記時刻復帰回路の情報にしたがって指針を早送り修正をすることを特徴とする請求項１記載の指針式電子時計のデータ送受信システム。

【請求項３】　前記時刻復帰回路は機能モードを設定するタイマ手段を設け、該タイマ手段の動作終了信号により前記時刻復帰回路が動作して指針を早送り修正をする請求項２記載の指針式電子時計のデータ送受信システム。

【請求項４】　発振回路と、該発振回路の出力信号の周波数を調整する歩度調整手段と、該歩度調整手段の歩度調整データを記憶する歩度調整データ記憶手段と、指針駆動パルスを発生する駆動信号発生回路と、変換機駆動回路と、該変換機駆動回路の出力信号によって駆動される変換機用コイルとを備えた指針式電子時計と、該指針式電子時計の変換機用コイルより発生する周期性を有する基準電磁信号を検出して歩度測定を行ない、その測定結果より指針式電子時計の歩度調整データを作成し、その歩度調整データを調整電磁信号として前記指針式電子時計に出力する歩度調整装置とにより構成される歩度調整システムであって、前記指針式電子時計は歩度測定用パルスを発生する歩度信号発生回路と、該歩度信号発生回路と前記駆動信号発生回路とを前記変換機駆動回路に対して切り替え接続するための切替回路と、該切替回路を制御するための歩度測定指定端子とを備えたことをことを特徴とする指針式電子時計のデータ送受信システム。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は、指針式電子時計のデータ送受信システムに関するものである。

【０００２】

【従来の技術】従来、電子時計に於ける設定機能の一例

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として歩度調整機能があるが、この歩度調整方法は電子時計から出力される歩度信号の周期を測定して、基準周期との差を歩度調整量としてその歩度調整量を外部から入力端子を用いてデジタル的に供給し、不揮発性メモリ等で構成されるメモリ回路に記憶させているものが主流である。又指針式電子時計においては指針駆動用の変換機用コイルを兼用して信号の受信を行なうデータ受信システムの一例として外部の標準時間信号発生装置から標準時間信号を受信して歩度調整を行なう指針式電子時計が提案されている。（例えば、特公昭５８－７１９０号公報）この時計は外部からの１秒周期の標準時間信号を受信するために、リューズ等外部操作部材の操作により受信状態を設定し、同時に分周回路をリセット状態にして標準時間信号が入力されるのを待つ。１発目の標準時間信号が入力されると分周回路のリセットが解除され、周波数偏差測定回路がカウントを開始する。そして１秒後に２発目の標準時間信号が入力されるとカウントを停止するとともに前記周波数偏差測定回路がカウントした周波数偏差を周波数偏差記憶回路に記憶させて自動歩度調整を終了する。そして、再度リセットがかけられ一定時間後自動的にリセットが解除されて通常動作が開始されるようにしたものである。すなわち上記動作においては外部から供給される正確な１秒周期の標準時間信号を内部カウンタで計数し、その計数値を以後の１秒の周期として計時動作を行なう一方的な受信方式であり、その標準時間信号の受信に変換機用コイルを利用しているものである。

【０００３】

【発明が解決しようとする課題】上記方式は、完成時計においても歩度調整を行なう事ができ大変便利な方式である。しかし、この歩度調整方式は指針式電子時計の歩度に関係なく外部の標準時間信号発生装置から例えば１秒間隔の標準時間信号を一方的に送り込み、指針式電子時計側では受信した１秒間隔信号を内蔵する発振回路の周波数によって計数し、その計数値を記憶しておき以後その計数値によって１秒信号を作成するという一方向性の書き込み方式である。しかるに上記方式では歩度調整データの記憶手段として１秒間の計数値に対応した多くのメモリを必要とするため小型で低消費電流が必要とされる腕時計においては採用されていない。現在電子腕時計で採用されている歩度調整手段としては少ないメモリ容量を用いて可変分周を行なったり発振回路の容量を時分割で切替える方式が採用されている。また標準時間信号を受信するためにリューズ等外部操作部材の操作により受信状態を設定し、同時に分周回路をリセット状態にするため、時計としての動作が停止状態となる。従って、歩度調整を行った後に再度時刻合わせをする必要がある。本発明の目的は電子時計からのタイミング信号を同期信号として双方向通信を行なう指針式電子時計のデータ送受信システムを提供する。かつ受信状態にて発生

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する指針駆動パルスを記憶し受信終了後に早送り修正を行ない時刻修正を不要にした指針式電子時計のデータ送受信システムを提供する。さらに上記の少容量メモリを用いた歩度調整手段に適応可能なデータ送受信システムを提供するものである。

【０００４】

【課題を解決するための手段】上記の目的を達成させるため、本発明は次の様な構成としている。データ信号を発生するデータ送信装置と、指針駆動用の変換機用コイルを兼用して前記データ送信装置からのデータ信号を受信する電子時計より構成される電子時計のデータ送受信システムに於て、前記電子時計にはタイミング信号を発生するタイミング信号発生手段と、指針駆動パルスを発生する駆動信号発生回路と、変換機駆動回路と、前記タイミング信号発生手段と前記駆動信号発生回路とを前記変換機駆動回路に対して切り替え接続するための切替回路と、該切替回路を制御するための機能設定用端子とを備え前記機能設定用端子によって前記切替回路を制御して機能モードを設定している間変換機用コイルを兼用し、かつ前記タイミング信号を同期信号として送受信動作を行うことを特徴とする。

【０００５】さらに、前記切替回路が機能モードを設定している間に発生する指針駆動パルスを記憶する時刻復帰回路を設け、前記切替回路が時刻モード復帰時に前記時刻復帰回路の情報にしたがって指針を早送り修正をすることを特徴とする。

【０００６】さらに、前記時刻復帰回路は機能モードを設定するタイマ手段を設け、該タイマ手段の動作終了信号により前記時刻復帰回路が動作して指針を早送り修正をすることを特徴とする。

【０００７】さらに、発振回路と、該発振回路の出力信号の周波数を調整する歩度調整手段と、該歩度調整手段の歩度調整データを記憶する歩度調整データ記憶手段と、指針駆動パルスを発生する駆動信号発生回路と、変換機駆動回路と、該変換機駆動回路の出力信号によって駆動される変換機用コイルとを備えた指針式電子時計と、該指針式電子時計の変換機用コイルより発生する周期性を有する基準電磁信号を検出して歩度測定を行ない、その測定結果より指針式電子時計の歩度調整データを作成し、その歩度調整データを調整電磁信号として前記指針式電子時計に出力する歩度調整装置とにより構成される歩度調整システムであって、前記指針式電子時計は歩度測定用パルスを発生する歩度信号発生回路と、該歩度信号発生回路と前記駆動信号発生回路とを前記変換機駆動回路に対して切り替え接続するための切替回路と、該切替回路を制御するための歩度測定指定端子とを備えたことをことを特徴とする。

【０００８】

【実施例】以下図面により本発明の送受信システムを歩度調整機能に適応した実施例を説明する。図１は本発明

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における第一実施例を示す歩度調整機能を備えた指針式電子時計の歩度調整システムのブロック図である。１は指針を駆動するための変換機用コイル１５ａと指針駆動を停止して時刻を修正するためのリューズ２４に連動して作動する修正スイッチＲＳを備えた指針式電子時計である。２は歩度調整装置であり、送受信用コイル３１を備えている。前記送受信用コイル３１は前記変換機用コイル１５ａとの間で送受信を行なう。前記歩度調整装置２は前記指針式電子時計１の時刻修正時に変換機用コイル１５ａから発生する基準電磁信号Ｓ４０を前記送受信用コイル３１で受信して歩度測定を行ない、その測定結果より指針式電子時計１の歩度調整データを作成し、前記基準電磁信号Ｓ４０に同期して前記歩度調整データを調整電磁信号４１として前記変換機用コイル１５ａに送信する様構成されている。

【０００９】図２は本発明における指針式電子時計１の回路ブロック線図である。１１は水晶振動子を基準信号とする発振回路であり、１２は発振回路１１からの発振信号を入力として指針駆動パルスを作成するための１Ｈｚ信号及び分周信号Ｓ１を出力する分周回路である。１３は駆動信号発生回路であり、分周回路１２からの１Ｈｚ信号を入力としモータを駆動する信号として変換機駆動回路１４に指針駆動用パルスＰＭを出力する。１５ａは指針駆動装置２３を駆動するための変換機１５に備えられた変換機用コイルであり前記歩度調整装置２との送受信を行なう送受信用コイルとしての機能を有する。２４は指針駆動装置２３の時刻を修正するためのリューズであり通常状態では０段の位置にある。スイッチＲＳはリューズ２４を１段引くことにより連動して作動する修正スイッチであり、歩度測定指定端子としての機能を有し、駆動信号発生回路１３からの指針駆動用パルスＰＭ出力を禁止する。２５は歩度信号発生回路であり、分周回路１２からの１Ｈｚ信号を入力とし１秒周期でかつパルスモータが駆動されない程度のパルス幅の歩度測定用パルスＰＨを変換機駆動回路１４に出力する。

【００１０】２６は指針駆動用パルスＰＭと歩度測定用パルスＰＨを入力とし、通常状態では指針駆動用パルスＰＭを選択し、リューズ２４を１段引いた修正状態では歩度測定用パルスＰＨを選択して変換機駆動回路１４に出力する切替回路である。本実施例においては歩度信号発生回路２５から出力される歩度測定用パルスＰＨが前記歩度調整装置２へ送信されるタイミング信号となり、従って歩度信号発生回路２５がタイミング信号発生回路としての機能を兼ね備えるものである。前記変換機用コイル１５ａは歩度測定用パルスＰＨが供給されると基準電磁信号Ｓ４０を発生する。１６は制御信号発生回路であり、前記分周信号Ｓ１を入力して、前記変換機駆動回路１４を受信状態にする受信可能信号Ｓ２等の多くの制御信号を出力する。１７は検出許可回路であり前記制御信号発生回路１６より出力される検出許可信号Ｓ３によ

って、調整電磁信号Ｓ４１を受信した変換機用コイル１５ａからの受信信号Ｓ１２の通過を禁止したり許可したりする。１８は歩度調整信号検出回路であり、前記検出許可回路１７を通過した受信信号Ｓ１２を歩度調整信号Ｓ４に変換する。１９はシフトレジスタであり、歩度調整信号検出回路１８からの歩度調整信号Ｓ４を前記制御信号発生回路１６より出力されるデータシフト信号Ｓ５により記憶し、データ信号Ｄ１、データ信号Ｄ２を出力する。

【００１１】２０は書換判定回路であり、前記制御信号発生回路１６より出力されるデータ判定信号Ｓ６により前記シフトレジスタ１９で記憶されたデータ信号Ｄ１が有効であるかを判定し、正しければ前記制御信号発生回路１６にデータ書換許可信号Ｓ７を出力する。２１は昇圧回路であり、前記制御信号発生回路１６より出力される消去信号Ｓ８、書込信号Ｓ９により昇圧動作を行ない一定時間だけ昇圧信号Ｓ１０を出力する。２２は不揮発性メモリ等で構成される歩度調整量記憶回路であり、前記シフトレジスタ１９からのデータ信号Ｄ２と昇圧回路２１からの昇圧信号Ｓ１０を入力とし、前記制御信号発生回路１６より出力される消去信号Ｓ８、書込信号Ｓ９によりデータの消去、書込が行なわれることにより、前記分周回路１２に歩度データＤ３を供給する。

【００１２】第３図は本発明における歩度調整装置２の回路ブロック線図であり、本実施例に於ける歩度調整装置２は前記指針式電子時計１からの基準電磁信号Ｓ４０を歩度検出信号として受信し、これに基づいて歩度測定を行ない、その結果に従う歩度調整データを調整電磁信号４１として送信する歩度調整装置である。３１は前記送受信用コイルである。３２は送受信切替回路であり、後述する送受信制御回路３９からの切替信号Ｓ２１により、前記変換機用コイル１５ａからの基準電磁信号Ｓ４０を受信したり、変換機用コイル１５ａへ調整電磁信号４１を送信したりすることを切替制御する。３３はゲート回路であり、前記基準電磁信号Ｓ４０の通過を禁止したり、許可したりする。３４は歩度信号検出回路であり、フィルタ回路３４ａと増幅回路３４ｂとで構成され、前記ゲート回路３３からの基準電磁信号Ｓ４０を入力し歩度検出パルスＰＴとして検出する。３５は周期測定回路であり前記歩度検出パルスＰＴを入力とし、複数の歩度検出パルスＰＴの間隔を基準信号発生回路３６からの基準信号Ｓ１３により測定し、測定データＤ４を出力する。

【００１３】３７は測定開始記憶回路であり、スイッチ３８の操作により歩度調整装置２を初期化するシステムクリア信号Ｓ２２を出力すると同時に受信許可信号Ｓ２３を出力し、前記ゲート回路３３が前記変換機用コイル１５ａからの基準電磁信号Ｓ４０の通過を許可するよう制御している。３９は送受信制御回路であり、前記歩度検出パルスＰＴを入力とし前記送受信切替回路３２を送

信状態にする切替信号Ｓ２１等の多くの制御信号を出力する。４７は第１データ記憶回路であり、前記周期測定回路３５からの測定データＤ４を入力とし、前記送受信制御回路３９が前記歩度検出パルスＰＴを入力する度に出力する周期ラッチ信号Ｓ３１により前記測定データＤ４を記憶し周期記憶データＤ８を出力する。４８は第２データ記憶回路であり、前記第１データ記憶回路４７からの周期記憶データＤ８を入力として、後述する比較判定回路４９より出力されるＮＧ信号Ｓ３４により前記周期記憶データＤ８を新たに記憶し周期基準データＤ９として出力する。４９は比較判定回路であり、前記周期記憶データＤ８と前記周期基準データＤ９を入力とし、前記送受信制御回路３９より出力される比較信号Ｓ３２により前記周期記憶データＤ８と前記周期基準データＤ９を比較判定し、比較した値が規格範囲内であればＯＫ信号Ｓ３３を前記送受信制御回路３９に出力し、比較した値が規格範囲外であればＮＧ信号Ｓ３４を第２データ記憶回路に出力する。

【００１４】４１は歩度調整量演算回路であり、前記周期記憶データＤ８を入力し前記送受信制御回路３９より出力される演算命令信号Ｓ２４により歩度調整量の演算が開始される。演算が終了すると調整量データＤ５を出力するとともに前記送受信制御回路３９に演算終了信号Ｓ２５を出力する。４２は送信データ作成回路であり、前記歩度調整量演算回路４１からの調整量データＤ５を入力し、バイナリコード形式のデータ信号Ｄ６に変換する。４３は書換コマンド作成回路であり、指針式電子時計１に対して、これからデータ信号Ｄ６を送信するという意味のデータ信号Ｄ７を作成する。４５は表示回路であり、前記歩度調整量演算回路４１からの調整量データＤ５を入力とし、基準値に対してｐｐｍ又は日差に変換する変換回路と、ＬＣＤ等を備えた表示装置４６を駆動する駆動回路で構成される。５０はＮＧ回数計数回路であり、前記比較判定回路４９より出力されるＮＧ信号Ｓ３４を入力し、カウントを行ないカウントが一定の回数以上（例えば５回）になるとリセット信号Ｓ３５を出力する。該リセット信号Ｓ３５は前記測定開始記憶回路３７および表示回路４５をクリアして初期化する。

【００１５】４４はデータ送信回路であり、前記データ信号Ｄ６、データ信号Ｄ７を入力とし前記送受信制御回路３９より出力されるラッチ信号Ｓ２６によりラッチし、後述するクロック発生回路４０から出力されるクロック信号Ｓ２７により前記データ信号Ｄ７とデータ信号Ｄ６を直列データ化した送信信号Ｓ２８を出力する。該送信信号Ｓ２８は前記送受信用コイル３１により調整電磁信号Ｓ４１として前記指針式電子時計１に送信される。４０はクロック発生回路であり、前記送受信制御回路３９より出力される起動信号Ｓ２９により前記データ送信回路４４を駆動するクロック信号Ｓ２７を出力する。又前記送受信制御回路３９より出力される送信終了

信号Ｓ３０は前記測定開始記憶回路３７をリセットして歩度調整装置２を初期化すると同時に前記ゲート回路３３が前記変換機用コイル１５ａからの基準電磁信号Ｓ４０の通過を禁止する。

【００１６】次に上記構成における歩度調整機能を備えた指針式電子時計１の歩度調整システムの動作を図４のタイムチャートに従って説明する。前記指針式電子時計１の通常動作はリューズ２４が０段の位置にあり前記切換回路２６はモータ駆動パルスＰＭを選択し出力する。該モータ駆動パルスＰＭを入力する変換機駆動回路１４は変換機駆動信号Ｓ１１を出力して変換機用コイル１５ａに供給することにより、変換機コイル１５ａが指針駆動装置２３を駆動して１秒運針にて時刻表示を行なう。修正状態ではリューズ２４が１段引きされリューズ２４に連動して作動する修正スイッチＲＳがＯＮ状態となり修正信号Ｓ１４を出力する。該修正信号Ｓ１４により前記駆動信号発生回路１３からの指針駆動用パルスＰＭ出力を禁止し、同時に前記切換回路２６は歩度測定用パルスＰＨを選択し出力する。該歩度測定用パルスＰＨを変換機用コイル１５ａに供給することにより、変換機用コイル１５ａより基準電磁信号Ｓ４０が発生する。前記制御信号発生回路１６は歩度測定用パルスＰＨが出力された後分周回路１２からの分周信号Ｓ１を入力して受信可能信号Ｓ２を出力することにより、歩度調整装置２からの調整電磁信号Ｓ４１を変換機用コイル１５ａで受信できるように変換機駆動回路１４を受信状態に切替える。同時に前記制御信号発生回路１６は検出許可信号Ｓ３を出力し検出許可回路１７に受信信号Ｓ１２の通過を許可する。これで指針式電子時計１は最初の歩度測定用パルスＰＨを基準電磁信号Ｓ４０として出力した後、次の歩度測定用パルスＰＨ出力までの間に受信可能信号Ｓ２の時間だけ受信可能状態に保持される。

【００１７】一方歩度調整装置２は前記指針式電子時計１の基準電磁信号Ｓ４０を受信するために、先ずスイッチ３８の操作にて初期化を行なう。該スイッチ３８の操作により前記測定開始記憶回路３７はシステムクリア信号Ｓ２２および受信許可信号Ｓ２３を出力する。システムクリア信号Ｓ２２により、送受信切替回路３２が受信モードを切替えられ、前記指針式電子時計１からの基準電磁信号Ｓ４０を受信することができる受信状態にする。同時に、システムクリア信号Ｓ２２によって前記書換コマンド作成回路４３はデータ信号Ｄ７を作成して出力する。同時に前記周期測定回路３５、前記第２データ記憶回路４８およびＮＧ回数計数回路５０をクリアする。さらに前記測定開始記憶回路３７からの受信許可信号Ｓ２３は、ゲート回路３３を制御して前記送受信用コイル３１からの基準電磁信号Ｓ４０の通過を許可する。この状態で前記指針式電子時計１の基準電磁信号Ｓ４０が受信されると、受信信号はゲート回路３３を通過して歩度信号検出回路３４に入力され、該歩度信号検出回路３４は最初の基準電磁信号Ｓ４０である歩度検出パルスＰＴを検出する。（図４タイムチャートｔ１のタイミング）

【００１８】周期測定回路３５は最初の歩度検出パルスＰＴ１が入力された時点ｔ１で今までカウントしていた基準信号発生回路３６からの基準信号Ｓ１３のカウントを終了し、測定データＤ４（最初の値は正しくない）として出力し再度カウントを開始する。同時に前記送受信制御回路３９は歩度検出パルスＰＴ１を入力すると周期ラッチ信号Ｓ３１を出力する。該周期ラッチ信号Ｓ３１により前記第１データ記憶回路４７は前記周期測定回路３５がカウントを終了した時点の測定データＤ４を記憶し周期記憶データＤ８を出力する。次に前記送受信制御回路３９は比較信号Ｓ３２を出力する。該比較信号Ｓ３２により前記比較判定回路４９は前記周期記憶データＤ８と第２データ記憶回路４８から出力される前記周期基準データＤ９（最初の値は０である）を比較し、ＮＧ信号Ｓ３４を出力する。該ＮＧ信号Ｓ３４により第２データ記憶回路４８は前記周期記憶データＤ８を新たな周期基準データＤ９として記憶する　。同時に前記ＮＧ回数計数回路５０は、前記比較判定回路４９より出力されるＮＧ信号Ｓ３４をカウントしカウント回数が１となる。

【００１９】次に指針式電子時計１から次の基準電磁信号Ｓ４０が出力され、この基準電磁信号Ｓ４０が前記送受信用コイル３１によって受信されることにより前記歩度信号検出回路３４から２番目の歩度検出パルスＰＴ２が出力される（図４タイムチャートｔ２のタイミング）と、周期測定回路３５は最初の歩度検出パルスＰＴ１が入力された時点ｔ１からカウントしていた基準信号Ｓ１３のカウントを終了し、測定データＤ４（図４タイムチャートｔ１とｔ２の周期Ｔ１）として出力し再度カウントを開始する。同時に前記送受信制御回路３９は歩度検出パルスＰＴ２を入力すると周期ラッチ信号Ｓ３１を出力する。該周期ラッチ信号Ｓ３１により前記第１データ記憶回路４７は前記周期測定回路３５がカウントを終了した時点の測定データＤ４（Ｔ１）を記憶し周期記憶データＤ８（Ｔ１）を出力する。次に前記送受信制御回路３９は比較信号Ｓ３２を出力し、該比較信号Ｓ３２により前記比較判定回路４９は前記周期記憶データＤ８と第２データ記憶回路４８から出力される前記周期基準データＤ９を比較し、ＮＧ信号Ｓ３４を出力する。該ＮＧ信号Ｓ３４により第２データ記憶回路４８は前記周期記憶データＤ８を新たな周期基準データＤ９（Ｔ１）として記憶し、同時に前記ＮＧ回数計数回路５０は、前記比較判定回路４９より出力されるＮＧ信号Ｓ３４をカウントしカウント回数が２となる。

【００２０】さらに指針式電子時計１から基準電磁信号Ｓ４０が出力され、この基準電磁信号Ｓ４０が前記送受信用コイル３１によって受信されることにより前記歩度信号検出回路３４から３番目の歩度検出パルスＰＴ３が

出力される（図４タイムチャートｔ３のタイミング）と、周期測定回路３５は歩度検出パルスＰＴ２が入力された時点ｔ２からカウントしていた基準信号Ｓ１３のカウントを終了し、測定データＤ４（図４タイムチャートｔ２とｔ３の周期Ｔ２）として出力し再度カウントを開始する。同時に前記送受信制御回路３９は歩度検出パルスＰＴ３を入力すると周期ラッチ信号Ｓ３１を出力する。該周期ラッチ信号Ｓ３１により前記第１データ記憶回路４７は前記周期測定回路３５がカウントを終了した時点の測定データＤ４（Ｔ２）を記憶し周期記憶データＤ８（Ｔ２）を出力する。次に前記送受信制御回路３９は比較信号Ｓ３２を出力し、該比較信号Ｓ３２により前記比較判定回路４９は前記周期記憶データＤ８（Ｔ２）と第２データ記憶回路４８から出力される前記周期基準データＤ９（Ｔ１）を比較し、比較した値が規格範囲内なのでＯＫ信号Ｓ３３が前記送受信制御回路３９に出力され前記送受信制御回路３９は演算命令信号Ｓ２４を出力する。

【００２１】該演算命令信号Ｓ２４が歩度調整量演算回路４１に出力されると歩度調整量演算回路４１は前記周期記憶データＤ８（Ｔ２）から歩度調整量の演算を開始し、演算が終了すると演算結果である調整量データＤ５を出力するとともに前記送受信制御回路３９に演算終了信号Ｓ２５を出力する。前記歩度調整量演算回路４１から出力された調整量データＤ５は送信データ作成回路４２でバイナリコード形式のデータ信号Ｄ６に変換される。又調整量データＤ５は同時に表示回路４５で日差に変換されその値が表示装置４６に表示される。前記演算終了信号Ｓ２５が前記送受信制御回路３９に出力されると送受信制御回路３９はラッチ信号Ｓ２６を出力し、前記データ信号Ｄ７およびデータ信号Ｄ６をデータ送信回路４４に記憶する。また前記歩度検出パルスＰＴ３に同期して切替信号Ｓ２１を出力（図４タイムチャートｔ４）し、送受信切替回路３２を送信状態に設定する。そして送受信制御回路３９から次に出力される起動信号Ｓ２９によって動作するクロック発生回路４０からのクロック信号Ｓ２７によって、データ送信回路４４に記憶されているデータ信号Ｄ７およびデータ信号Ｄ６を送信信号Ｓ２８として順次出力する。送信信号Ｓ２８は送受信切替回路３２、送受信用コイル３１を介して前記指針式電子時計１へ調整信号Ｓ４１として送信される。送信信号Ｓ２８を全て送信し終わると送受信制御回路３９は送信終了信号Ｓ３０を出力する。

【００２２】前記一連の送信信号Ｓ２８が送信されるタイミングは図４のタイムチャートの切替信号Ｓ２１と前記指針式電子時計１の受信可能信号Ｓ２に示すごとく指針式電子時計１の制御信号発生回路１６が受信可能信号Ｓ２を出力している状態すなわち指針式電子時計１の受信状態に合っている。前記送受信制御回路３９からの送信終了信号Ｓ３０は前記測定開始記憶回路３７に入力さ

れ、該測定開始記憶回路３７がリセットされることにより受信許可信号Ｓ２３が停止し、前記ゲート回路３３を閉じられる。以上で１回の歩度調整動作が終了し、再度歩度調整動作を行ないたい場合はスイッチ３８を押すことによって再開される。

【００２３】一方前記歩度調整装置２より送信された調整磁気信号Ｓ４１は、指針式電子時計１の変換機用コイル１５ａによって受信される事になるが、以下その動作を説明する。前記指針式電子時計１は制御信号発生回路１６が出力する受信可能信号Ｓ２で、変換機駆動回路１４を受信状態に切替えて、歩度調整装置２から送信されるデータ信号Ｄ７とデータ信号Ｄ６で構成された調整磁気信号Ｓ４１を変換機用コイル１５ａで受信信号Ｓ１２として受信する。受信した受信信号Ｓ１２は検出許可回路１７を介して歩度調整信号検出回路１８にて検出され歩度調整信号Ｓ４として出力される。検出された歩度調整信号Ｓ４は制御信号発生回路１６が出力するデータシフト信号Ｓ５でシフトレジスタ１９に順次記憶され、歩度調整信号Ｓ４の記憶が全て終了すると、前記データ信号Ｄ７をデータ信号Ｄ１として前記書換判定回路２０へ出力し、前記データ信号Ｄ６をデータ信号Ｄ２として前記歩度調整記憶回路２２へ出力する。制御信号発生回路１６はデータシフト信号Ｓ５を出力し終わるとデータ判定信号Ｓ６を前記書換判定回路２０へ出力し、該書換判定回路２０はデータ信号Ｄ１が有効であるかを判定し、有効であればデータ書換許可信号Ｓ７を出力する。しかし、前記書換判定回路２０での判定結果が無効のときはデータ書換許可信号Ｓ７が出力されず歩度調整は行なわれない。

【００２４】制御信号発生回路１６はデータ書換許可信号Ｓ７が入力されると消去信号Ｓ８を出力し、歩度調整量記憶回路２２を消去モードに設定し同時に昇圧回路Ｓ２１を動作させ昇圧信号Ｓ１０により歩度調整量記憶回路２２のデータを消去する。続いて制御信号発生回路１６は書込信号Ｓ９を出力し、歩度調整量記憶回路２２を書込モードに設定し同時に昇圧回路２１を動作させ昇圧信号Ｓ１０により調整量データであるデータ信号Ｄ２を歩度調整量記憶回路２２に書込むことにより歩度調整が終了する。

【００２５】図５は本発明における第二実施例の指針式電子時計１の回路ブロック線図である。本実施例は通常運針状態から指針の駆動を停止させてデータ送信装置からのデータ信号を一定時間受信できる受信可能状態を設定し、一定時間経過後受信可能状態から通常運針状態へ自動復帰させ、かつ自動復帰後に受信可能状態にて停止していた指針を早送り修正する自動復帰回路５３を設けることにより時刻合わせを不要にしたものであり、図２と同一要素には同一番号を付し、説明を省略する。ＲＳは前記リューズ２４に連動して作動する修正スイッチであり、機能設定用端子としての機能を有する。５２は発

振回路１１からの発振信号を入力として１Ｈｚ信号、早送り信号Ｓ５３及び分周信号Ｓ１を出力する分周回路である。５１はモード記憶回路であり、前記修正スイッチＲＳがＯＮ状態になると動作するワンショット回路５０からのワンショット信号Ｓ５９を入力して通常状態である早送りモードから受信モードへモードを切換設定し、受信モード信号Ｓ５１を出力する。制御信号発生回路６０は受信モード信号Ｓ５１が入力されることにより受信可能信号Ｓ２および検出許可信号Ｓ３を出力し指針式電子時計１を受信可能状態にする。

【００２６】５３は自動復帰回路であり、前記モード記憶回路５１から受信モード信号Ｓ５１が出力されている間指針駆動パルスＰＭを作成するための前記１Ｈｚ信号をカウント、記憶する。そして前記１Ｈｚ信号が所定の回数入力されたら前記モード記憶回路５１を通常状態の早送りモードに切り換える自動復帰信号Ｓ５４を出力する。前記モード記憶回路５１が切り換えられることによって早送りモード信号Ｓ５２が出力されると前記自動復帰回路５３は早送り信号Ｓ５３にて記憶した１Ｈｚ信号に一致するまでカウントし、同時に早送り信号Ｓ５３に同期して早送り駆動用パルスＰＦを出力する。５４はＯＲ回路であり、前記指針駆動用パルスＰＭと早送り駆動用パルスＰＦを入力し指針駆動信号Ｓ６０を出力する。

【００２７】次に上記構成における指針を早送り修正する自動復帰回路５３を備えた指針式電子時計１のデータ送受信システムの動作を図６のタイムチャートに従って説明する。修正スイッチＲＳがＯＦＦ状態の時は変換機駆動回路１４は分周回路５２からの１Ｈｚ信号を入力して指針駆動用パルスをＰＭ１出力する。（図６タイムチャートｔ５）次に前記リューズ２４が１段に引かれ修正スイッチＲＳがＯＮするとモード記憶回路５１から受信モード信号Ｓ５１が出力される。（図６タイムチャートｔ６）該受信モード信号Ｓ５１により制御信号発生回路６０は受信可能信号Ｓ２および検出許可信号Ｓ３を出力し指針式電子時計１を受信可能状態にするとともに自動復帰回路５３は前記１Ｈｚ信号をカウント開始する。前記自動復帰回路５３は所定の回数（ここでは４回）１Ｈｚ信号をカウントすると自動復帰信号Ｓ５４を出力し、該自動復帰信号Ｓ５４によりモード記憶回路５１は早送りモードに切り換えられ早送りモード信号Ｓ５２を出力する。（図６タイムチャートｔ７）自動復帰回路５３は早送りモード信号Ｓ５２により前記早送り信号Ｓ５３にて記憶した１Ｈｚ信号の回数（４回）に一致するまでカウントし、同時に早送り信号Ｓ５３に同期して早送り駆動用パルスＰＦを出力する。（図６タイムチャートｔ７－ｔ８間）早送り駆動用パルスＰＦはＯＲ回路５４を通過して指針駆動信号Ｓ６０となり早送り修正を行う。

【００２８】図７は図５における自動復帰回路５３の具体的な回路構成図であり以下のように構成されている。５３ａは１Ｈｚ信号の通過を許可する第１ゲート回路、

５３ｂは早送り信号Ｓ５３の通過を許可する第２ゲート回路である。５３ｄは１Ｈｚ信号記憶回路であり、前記第１ゲート回路５３ａを通過した１Ｈｚ信号をカウントし、１Ｈｚ信号記憶情報Ｓ５８を出力する。５３ｃは１Ｈｚ信号記憶情報Ｓ５８を入力とし、１Ｈｚ信号が所定の回数入力されたら前記モード記憶回路５１へ自動復帰信号Ｓ５４を出力するタイマ回路である。５３ｆは早送り駆動信号発生回路であり、前記第２ゲート回路５３ｂを通過した早送り信号Ｓ５２が入力される毎に前記早送り駆動パルス用ＰＦを出力し、同時に早送り信号Ｓ５２をカウントし、早送り情報Ｓ５７を出力する。５３ｅは１Ｈｚ信号記憶情報Ｓ５６と早送り情報Ｓ５７を入力して比較する比較回路であり、比較して一致していれば一致信号Ｓ５５を出力し、前記第２ゲート回路５３ｂを制御して早送り信号Ｓ５２の通過を禁止する。５３ｇは前記比較回路５３ｅからの一致信号Ｓ５５を入力し、ワンショットのクリア信号Ｓ５６を出力するクリア信号発生回路であり、前記クリア信号Ｓ５６は１Ｈｚ信号記憶回路５３ｄおよび早送り駆動信号発生回路５３ｆを初期化して早送り修正を終了する。

【００２９】図８は本発明の図２に示す指針式電子時計１における変換機駆動回路１４の回路構成図である。Ｔｐ１、Ｔｐ２、Ｔｎ１、Ｔｎ２は駆動用ＭＯＳトランジスタであり、前記駆動信号発生回路１３から出力されるモータ駆動パルスＰＭによって制御される。ＤＩ１、ＤＩ２はダイオードであり、前記変換機用コイル１５ａが受信した受信信号をクランプ整形し、前記検出許可回路１７へ出力する。次に上記構成を有する変換機駆動回路１４の動作を説明する。通常運針状態ではＴｐ１、Ｔｎ２がＯＦＦ、Ｔｎ１、Ｔｐ２がＯＮあるいはＴｎ１、Ｔｐ２がＯＦＦ、Ｔｐ１、Ｔｎ２がＯＮの時に変換機用コイル１５ａのＡ点とＢ点間に電圧が供給されて運針動作が行なわれる。又通常状態においてはＴｐ１、Ｔｐ２がＯＦＦ、Ｔｎ１、Ｔｎ２がＯＮであり、変換機用コイル１５ａのＡ点、Ｂ点にはＶｓｓが印加されている。この状態で前記制御信号発生回路１６から受信可能信号Ｓ２が入力されると、Ｔｎ１がＯＮ、Ｔｎ２、Ｔｐ１、Ｔｐ２がＯＦＦになり、変換機用コイル１５ａはＡ点がＧＮＤ（Ｖｓｓ電位）に落ちＢ点が浮いた状態になるので変換機用コイル１５ａは受信コイルの機能となって前記送受信装置２からの送信信号Ｓ２８を受けることができる。Ｂ点に発生した受信信号はダイオードＤＩ１、ＤＩ２でクランプ整形され、前記検出許可回路１７に送られる。

【００３０】尚、本発明においては自動復帰信号Ｓ５４により受信モードから通常状態の早送りモードに切り換えているが修正スイッチＲＳのＯＮ状態からＯＦＦ状態への操作によって復帰動作を行わせることも可能である。また歩度測定用パルスＰＨを１Ｈｚにしているがこれに限定されるものではなく、歩度測定用パルスＰＨの

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周波数を高くすることによって歩度調整時間が短縮されることは明白である。また歩度測定指定端子としてリューズに連動して作動するスイッチを利用しているが単独の歩度測定指定端子を設けても良い。また分周回路に歩度調整データを供給して歩度調整を行う方式であるが、発振回路の発振信号を時分割に制御して歩度調整を行う方式でも可能であることは言うまでもない。さらに実施例として歩度調整機能について示したが、これに限定されるものではなく、温度調整等、指針式電子時計に於ける各種設定機能に応用できるものである。

【００３１】

【発明の効果】以上の説明で明らかなように本発明によれば、時計を止めてかつタイミング信号を同期信号として双方向通信を行なうことによってパルスモータ駆動の誘起電圧に邪魔されることなく安定した双方向通信を行なうことができる。さらに通信モードで時計を止めている間に発生する１Ｈｚ信号を記憶し通信モード終了後早修正しているため時計としての機能を損ねることなく双方向通信ができる。さらに本発明を歩度調整に適応することによってメモリ容量の少ない歩度調整システムを可能にすることができる。

【図面の簡単な説明】

【図１】本発明の第一実施例を示す歩度調整機能を備えた指針式電子時計と歩度調整装置とによる歩度調整システムのブロック図である。

【図２】図１の指針式時計のブロック線図である。

【図３】図１の歩度調整装置のブロック線図である。

【図４】本発明の第一実施例の動作を示すタイムチャート図である。

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【図５】本発明の第二実施例における指針式電子時計のブロック線図である。

【図６】本発明の第二実施例の動作を示すタイムチャート図である。

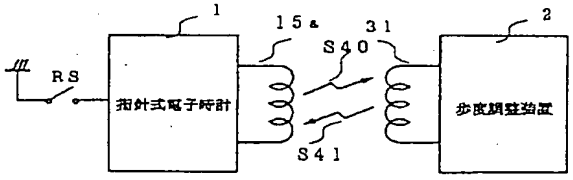
【図７】図６に於ける自動復帰回路５３の回路構成図である。

【図８】図１に於ける変換機駆動回路１４の回路構成図である。

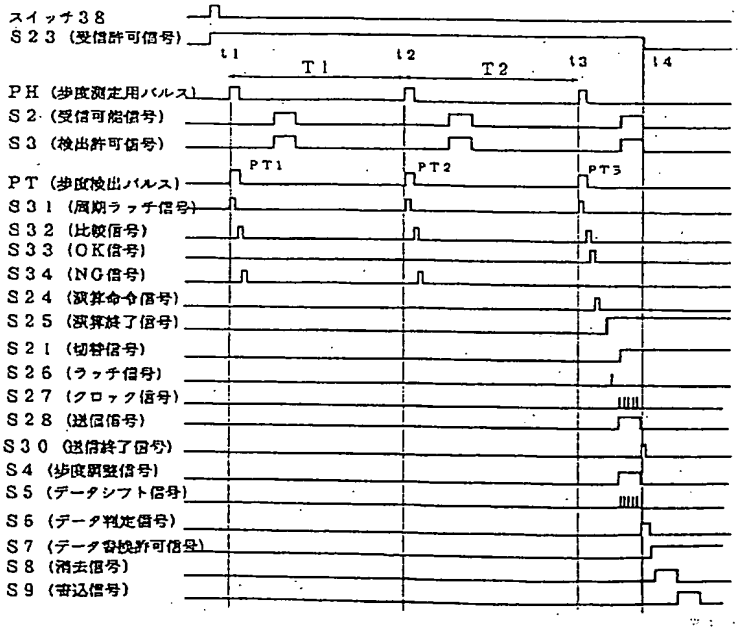
【符号の説明】

１　・・・指針式電子時計
２　・・・歩度調整装置
１３　・・・駆動信号発生回路
１６　・・・制御信号発生回路
１５ａ　・・・変換機用コイル
１８　・・・歩度調整信号検出回路
２０　・・・審換判定回路
２２　・・・歩度調整量記憶回路
２５　・・・歩度信号発生回路
２６　・・・切換回路
３１　・・・送受信用コイル
３２　・・・送受信切替回路
３４　・・・歩度信号検出回路
３９　・・・送受信制御回路
４４　・・・データ送信回路
５１　・・・モード記憶回路
５３　・・・自動復帰回路

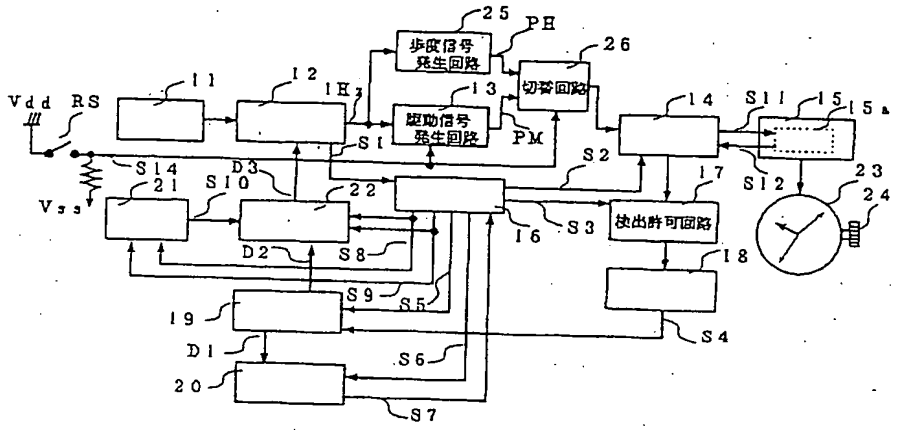
【図１】



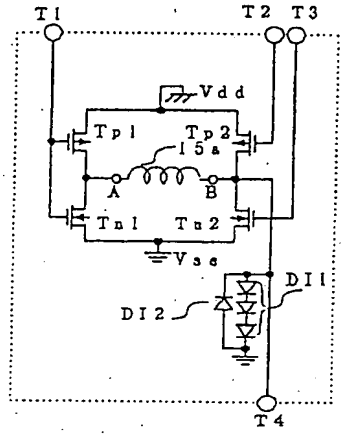
【図４】



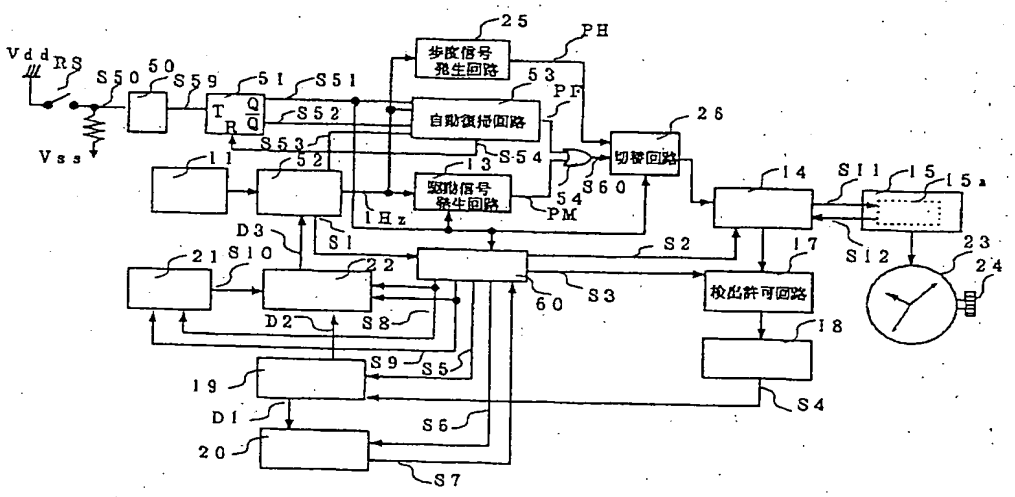
【図２】


歩度信号発生回路
駆動信号発生回路
切替回路
検出許可回路
Vdd
RS
Vss
PH
PM
1Hz
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S14
D1
D2
D3

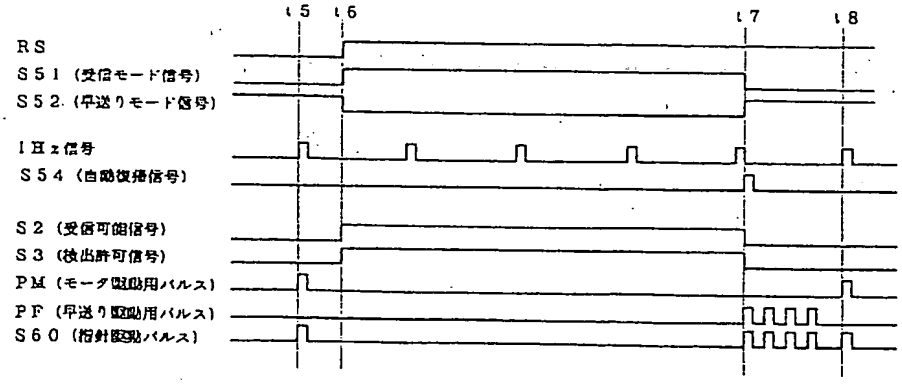
【図８】


T1
T2
T3
T4
Vdd
Tp1
Tp2
Tn1
Tn2
Vss
A
B
DI1
DI2

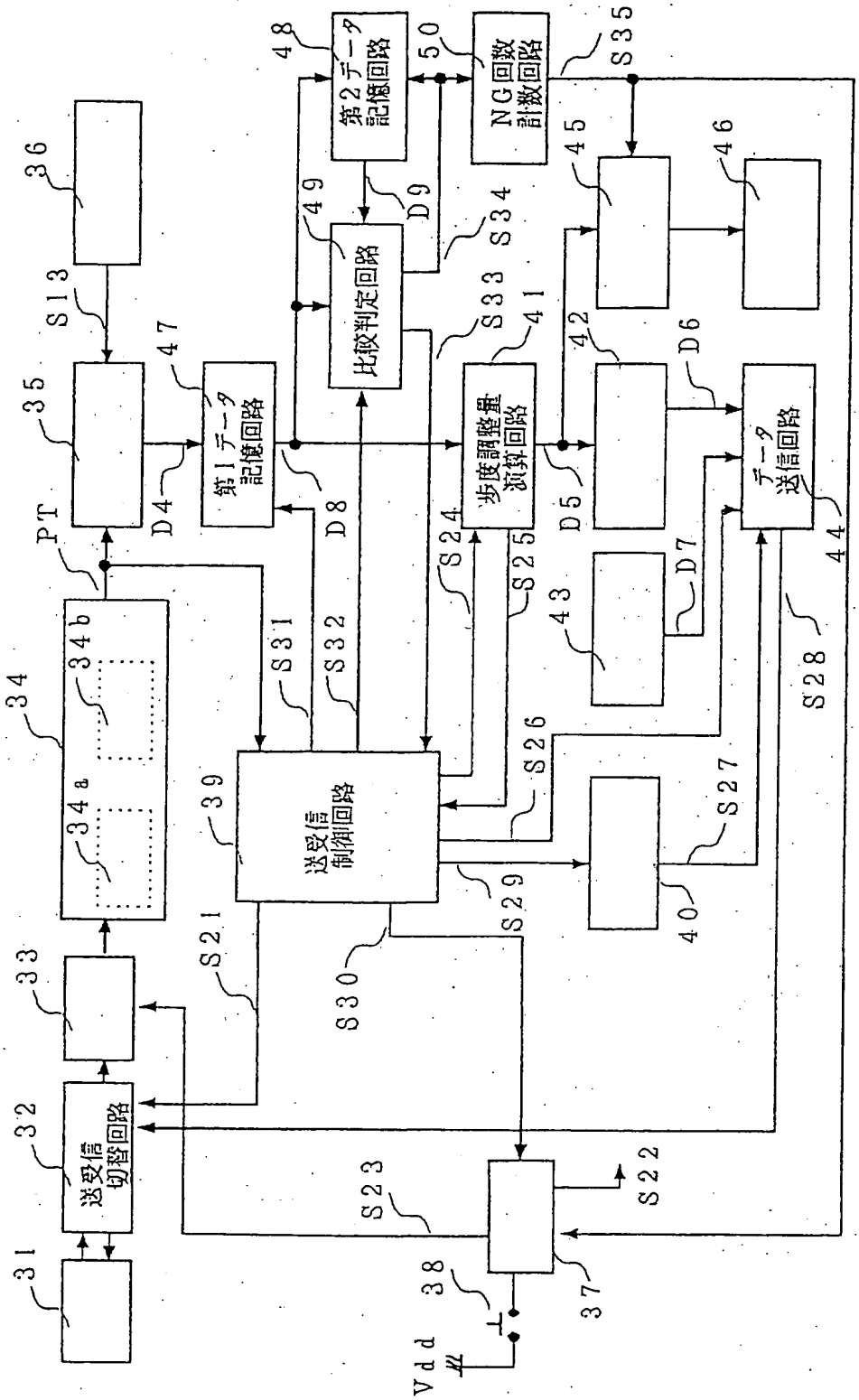
【図５】


歩度信号発生回路
駆動信号発生回路
自動復帰回路
切替回路
検出許可回路
Vdd
RS
Vss
PH
PM
PF
1Hz
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S50
S51
S52
S53
S54
S59
S60
D1
D2
D3

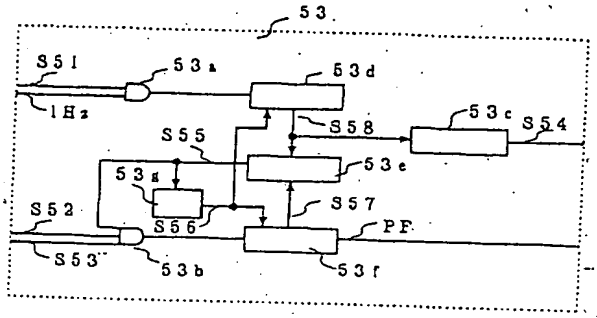
【図６】


t5
t6
t7
t8
RS
S51（受信モード信号）
S52（早送りモード信号）
1Hz信号
S54（自動復帰信号）
S2（受信可能信号）
S3（検出許可信号）
PM（モータ駆動用パルス）
PF（早送り駆動用パルス）
S60（指針駆動パルス）

【図3】


第2データ記憶回路
NG回数計数回路
比較判定回路
第1データ記憶回路
歩度調整量演算回路
データ送信回路
送受信制御回路
送受信切替回路
Vdd
PT
S13
S21
S22
S23
S24
S25
S26
S27
S28
S29
S30
S31
S32
S33
S34
S35
D4
D5
D6
D7
D8
D9
31
32
33
34
34a
34b
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50

【図７】


53
S51
53a
53d
1Hz
S58
53c
S54
S55
53e
53g
S52
S57
S56
PF
S53
53b
53f